

An All-Digital On-Chip Abnormal Temperature Warning Sensor for Dynamic Thermal Management

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Abstract—In this paper, an all-digital on-chip abnormal temperature warning sensor (ATWS) which can tolerate process and voltage variations after four-point calibration is presented. The proposed ATWS uses the delay ratios among three ring oscillators to build up a relative reference modeling (RRM) temperature sensor. Then the process variations can be eliminated after four-point calibration. In addition, the operational voltage can be estimated by the RRM. Thus, the proposed ATWS can use a linear model to compute the chip temperature even with voltage variations. The proposed ATWS is implemented in a 90nm CMOS process, and the active area is 0.0625mm^2 . It can achieve temperature error smaller than $\pm 3.66^\circ\text{C}$ within the range of 40°C to 70°C , and 0.9V to 1.1V . The power consumption is $530\mu\text{W}$ at 4k sample/s.

Keywords— Calibration, circuit reliability, dynamic thermal management, delay circuits, relative reference modeling, sensors.

I. INTRODUCTION

In recent years, the number of central processing units (CPUs) on a single embedded system has kept increasing and multiple chips are integrated and fabricated on a single chip. The power density becomes higher and causes the challenge of dark silicon in the multi-core system. Therefore, there are some localized high temperature areas called “hotspots.” Hotspots cause unusual temperature gradients across the chip and reduce the reliability of the chip. Thus, in system-on-a-chip (SoC) design, the dynamic thermal management (DTM) with many temperature warning sensors is very important for improving the reliability of the system.

Traditionally, the proportional-to-the-absolute-temperature (PTAT) pulse generators which created by a delay line or a ring oscillator are widely used in all-digital smart temperature sensors [2]-[4],[7]. Then, the reference clock or the time-to-digital converters (TDCs) are applied to quantize the pulse width into digital codes. After chip fabrication with one-point or two-point calibration, these digital codes can be converted to the temperature value in degree Celsius ($^\circ\text{C}$) by a linear equation. However, since the post-silicon calibration of the temperature sensor is at a fixed voltage, and thus, the slope and intercept of the linear equation will be changed with voltage variations. As a result, the output temperature error will be higher than expectation with voltage variations.

Fig. 1 shows the simulation results of the PTAT-based temperature sensor [2],[3]. The PTAT ring oscillator is composed of 20 inverters in series, and the number of the oscillation cycles to generate a PTAT pulse is set to $2^{14}-1$. In this simulation, an ideal TDC circuit is used to quantize the pulse width into digital codes. Then the two-point calibrations with a 1.0V power supply at different process corners are performed. As shown in Fig. 1, the error of the temperature sensor can be smaller than $\pm 1.7^\circ\text{C}$ with a 1.0V power supply at all process corners. However, when the PTAT-based temperature sensor suffers from voltage variations, the error of the temperature sensor can be as large as -268.4°C to $+175.3^\circ\text{C}$ at all process corners. Therefore, the PTAT-based temperature sensor [2]-[4],[7] has a good resolution and high accuracy at a fixed supply voltage, but it cannot tolerate voltage variations.

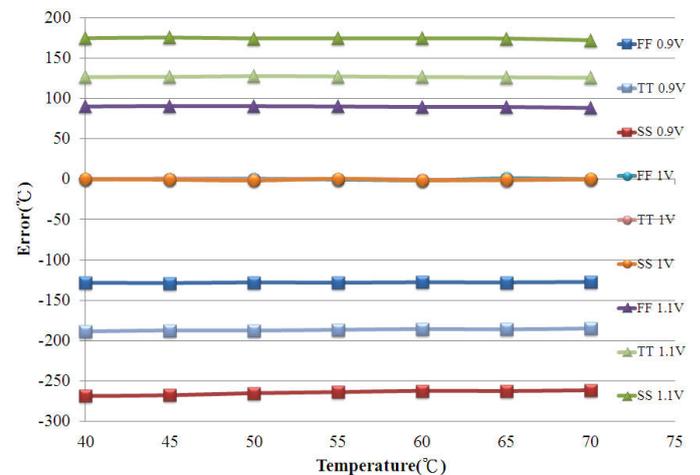


Fig. 1. The output temperature error of the PTAT-based temperature sensor with voltage and process variations.

If the calibrations of the temperature sensor are performed at different voltages, and then, the error of the temperature sensor can be greatly reduced. However, it needs to know the current operational voltage to choose a suitable linear equation for converting the digital codes into degree Celsius ($^\circ\text{C}$). The dual-DLL-based temperature sensor [5],[8] and the dual-ring-oscillator-based temperature sensor [6] can reduce the effects of process variations by relative comparison between two delay-lines or two ring oscillators. The two delay lines or two ring oscillators will both increase or decrease their output delay

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or output frequency at the same time with process variations, and thus, the temperature error can be reduced. However, as reported in [5],[8], they still cannot tolerate voltage variations. Thus, on-chip voltage regulators are usually needed for these temperature sensors, and the power and area consumption are increased accordingly.

In this paper, an all-digital on-chip abnormal temperature warning sensor (ATWS) which can tolerate process and voltage variations after four-point calibration is presented. The proposed ATWS uses the delay ratios between the three ring oscillators to build up a relative reference modeling (RRM). Then the proposed voltage classifier can estimate the current operational voltage and provide an accuracy linear model for the temperature calculator. As a result, the error of the temperature sensor with voltage variations can be greatly reduced.

The rest of the paper is organized as follows: Section II describes the system architecture of the proposed ATWS. The experimental results are discussed in Section III. Finally, Section IV concludes with a summary.

II. PROPOSED ATWS

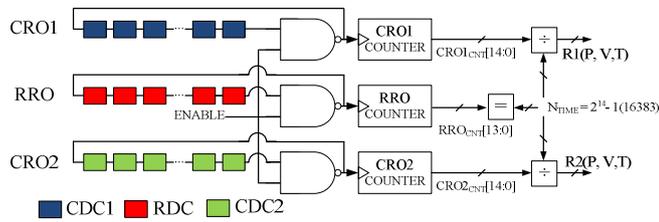


Fig. 2. The proposed delay ratio estimator.

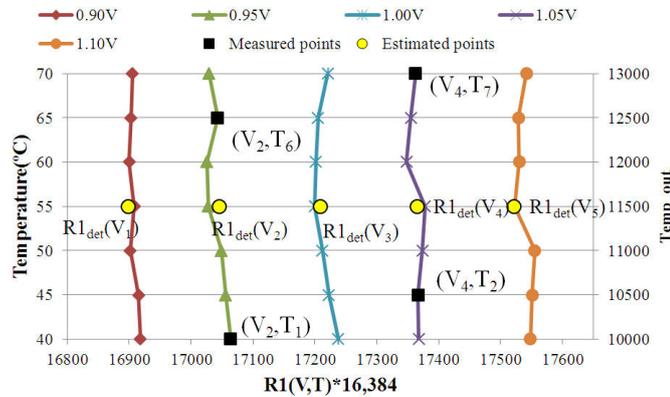


Fig. 3. Simulation results of the R1(V, T) at different voltage and temperature values.

Fig. 2 shows the block diagram of the proposed delay ratio estimator (DRE) [1]. In DRE, three logic cells, RDC, CDC1, and CDC2 are used to create three ring oscillators (RRO, CRO1, CRO2). The output of the ring oscillator is connected to the counter to record the oscillation cycles. The output value of these counters can be used to compute the delay ratios [9] $R1(P, V, T)$ and $R2(P, V, T)$ as defined in Eq. 1.

$$R1(P, V, T) = \frac{CRO1_{CNT}}{RRO_{CNT}}, \quad R2(P, V, T) = \frac{CRO2_{CNT}}{RRO_{CNT}} \quad (1)$$

where $CRO1_{CNT}$, $CRO2_{CNT}$, and RRO_{CNT} are the output of the CRO1 counter, CRO2 counter, and RRO counter, respectively. The RRO counter will count from 0 to N_{TIME} , and then, three ring oscillators are stopped to compute the delay ratios. The value of N_{TIME} is set to 16,383 to avoid using divider circuits.

Fig. 3 shows the simulation results of $R1(V, T)$ at typical process corner with different voltage and temperature values. The voltage value varies from V_1 to V_5 ($V_1=0.90V$, $V_2=0.95V$, $V_3=1.00V$, $V_4=1.05V$, and $V_5=1.10V$), and temperature value varies from T_1 to T_7 ($T_1=40^\circ C$, $T_2=45^\circ C$, $T_3=50^\circ C$, $T_4=55^\circ C$, $T_5=60^\circ C$, $T_6=65^\circ C$, and $T_7=75^\circ C$). We choose logic cells (CDC1, RDC) to make the $R1(P, V, T)$ curves at different voltage values to be non-overlapped in all process corners which means that we need to find two logic cells with similar temperature coefficients.

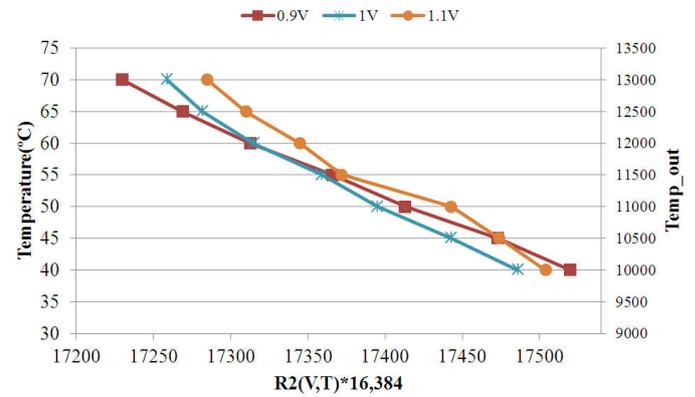


Fig. 4. Simulation results of the R2(V, T) at different voltage and temperature values.

Fig. 4 shows the simulation results of $R2(V, T)$ at typical process corner with different voltage and temperature values. We find two logic cells (CDC2, RDC) with different temperature coefficients. The output of the temperature sensor ($Temp_out$) can be expressed as a linear equation of $R2(V, T)$ in Eq. 2:

$$Temp_out = a(V_n) \times R2(V, T) + b(V_n) \quad (2)$$

After chip fabrication, we need to measure the DRE output values of $R1(V, T)$ and $R2(V, T)$ at four calibration points. The average value of $R1(V, T)$ at (V_2, T_1) and (V_2, T_6) is recorded as $R1_{det}(V_2)$. Similarly, the average value of $R1(V, T)$ at (V_4, T_2) and (V_4, T_7) is recorded as $R1_{det}(V_4)$. Subsequently, a linear interpolation and extrapolation are applied to compute $R1_{det}(V_n)$, where $n=1$ to 5. In addition, at different voltages, the $Temp_out$ will be linearly proportional to $R2(V, T)$. Thus, the slope $a(V_2)$ and the intercept $b(V_2)$ of the linear equation at $V_2=0.95V$ can be computed using the values of $R2(V, T)$ at two calibration points: (V_2, T_1) and (V_2, T_6) . Similarly, the values of $a(V_4)$ and $b(V_4)$ can be computed by the values of $R2(V, T)$ at two calibration points: (V_4, T_2) and (V_4, T_7) . Subsequently, a linear interpolation and extrapolation are applied to compute $a(V_n)$ and $b(V_n)$, where $n=1$ to 5. Then, $R1_{det}(V_n)$, $a(V_n)$ and

$b(V_n)$ which determined in the off-chip process are input to the proposed ATWS.

Fig. 5 shows the proposed all-digital on-chip abnormal temperature warning sensor (ATWS). It is composed of a delay ratio estimator (DRE), a voltage classifier, and a temperature calculator. At chip run time, the DRE computes $R1(V,T)$ and $R2(V,T)$. The voltage classifier uses the threshold values $R1_{det}(V_n)$ to determine the operation voltage. For example, as shown in Fig. 3, if $R1(V,T)$ is 17,200/16,384, then the value of $R1(V,T)$ is close to $R1_{det}(V_3)$. This means that the operational voltage is $V_3=1.00V$. The temperature calculator of the ATWS will use the slope $a(V_3)$ and the intercept $b(V_3)$ of the linear equation to compute the output temperature value.

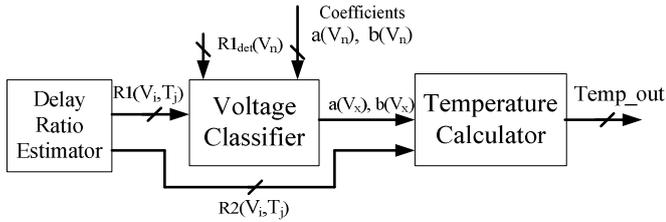


Fig. 5. The proposed abnormal temperature warning sensor.

III. EXPERIMENTAL RESULTS

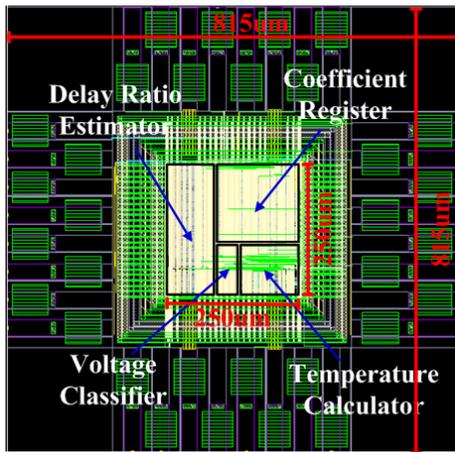


Fig. 6. Layout of the proposed ATWS.

The proposed ATWS is implemented in a standard performance (SP) 90nm 1P9M CMOS process. The layout of the ATWS is shown in Fig. 6. The operating voltage of the proposed ATWS ranges from 0.90V to 1.10V, and the operating temperature ranges from 40°C to 70°C. The active area is 250μm × 250μm, and the chip area including I/O pads is 815μm × 815μm.

After four-point calibration, Fig. 7 shows the simulation results of the proposed ATWS with process and voltage variations. The y-axis represents the temperature sensor output (°C) and the corresponding digital code (Temp_out). In Fig. 7, the line labeled “IDEAL” means the ideal temperature sensor output. The simulation results show that in different process corners and different voltages, the proposed ATWS is very close to the ideal line. In addition, the proposed ATWS outputs

a warning signal to the dynamic thermal management (DTM) circuit when the temperature value is within 40°C to 70°C. Then, the DTM circuit can stop some circuits or slow down the clock frequency of some circuits to avoid overheating the localized area of the chip.

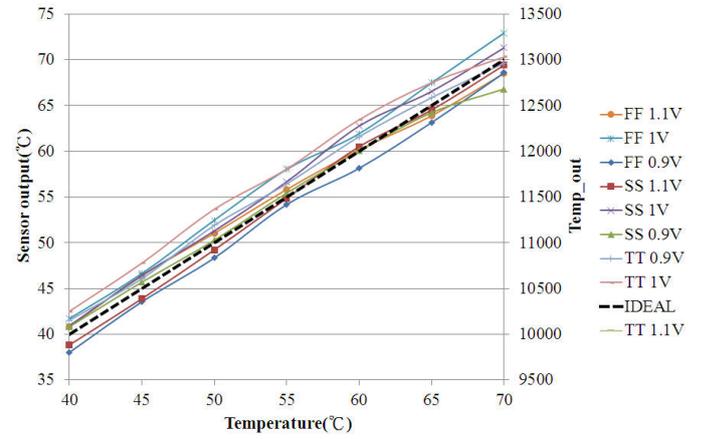


Fig. 7. The sensor output vs. operational temperature value at all process corners with voltage variations.

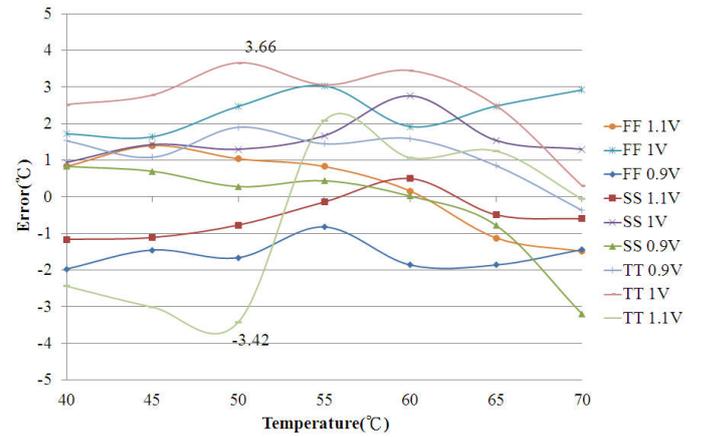


Fig. 8. Error of the proposed ATWS at all process corners with voltage variations.

Fig. 8 shows the temperature error of the ATWS with process and voltage variations. The output temperature error with process and voltage variations ranges from -3.42°C to +3.66°C, and the accuracy of the proposed ATWS is sufficient for dynamic thermal management applications.

Table I lists the comparisons of recent smart temperature sensors. In this table, the proposed ATWS is the only one temperature sensor which can tolerate voltage variations, but the proposed ATWS requires four-point calibration. The temperature sensor [7] with curvature compensation can achieve a very small temperature error 0.25°C ~ +0.35°C at 3.3V. However, when there has 10% voltage variations, the output error quickly increases to -10°C ~ +8°C. Similarly, the dual-DLL-based temperature sensor [5] achieves a temperature error -4°C ~ +4°C at 1.2V. However, when there has 10% voltage variations, the output error quickly increases to -90°C ~

TABLE I. PERFORMANCE COMPARISONS

Parameter	Proposed	[2] TCAS-II'11	[3] ISCAS'10	[4] TCAS-I'11	[5] TVLSI'12	[6] TVLSI'13	[7] JSSC'10
Type	three ring oscillators (all-digital)	PTAT (all-digital)	PTAT (all-digital)	PTAT (FPGA)	Dual-DLL (all-digital)	two ring oscillators	PTAT (all-digital)
VDD Range	0.9V ~ 1.1V	fixed 1.0V	fixed 1.0V	fixed 2.5V	fixed 1.2V	fixed 1.2V	3.0V ~ 3.6V
Resolution(°C)	0.168	0.139	0.143	0.133	0.78	0.34	0.0918
Error(°C)	-3.42 ~ +3.66 (with voltage variations)	-5.1 ~ +3.4 (at 1.0V)	~10 ~ +10 (at 1.0V)	-0.7 ~ +0.6 (at 2.5V)	-90 ~ +90 (with voltage variations) -4 ~ +4 (at 1.2V)	-2.8 ~ +2.9 (at 1.2V)	-10 ~ +8 (with voltage variations) -0.25 ~ +0.35 (at 3.3V)
Calibration Point	4 (with linear interpolation)	1	1	1 (with 2nd order curvature compensation)	1	1	2 (with curvature compensation)
Conversion Rate (samples/s)	4k	10k	10k	1k	5k	366k	2
Energy for one conversion (μJ)	0.1325	0.015	0.0055	0.175	0.24	0.00109	18.35
Power (μW)	530	150	55	175	1,200	400	36.7
Area(mm ²)	0.0625	0.01	0.01	N/A	0.12	0.0013	0.6
Range (°C)	40 ~ 70	0 ~ 60	0 ~ 100	0 ~ 100	0 ~ 100	-40 ~ 110	0 ~ 90
Technology(nm)	90	65	65	220	130	65	350

+90°C. In addition, the chip area and power consumption are too large in the dual-DLL-based temperature sensor [5]. The accuracy of current smart temperature sensors is sensitive to the voltage variations. Although these architectures [2]-[7] require one-point or two-point calibration, these architectures are not suitable for use as an on-chip temperature sensor for dynamic thermal management with localized voltage variations.

IV. CONCLUSION

In this paper, an all-digital on-chip abnormal temperature warning sensor (ATWS) which can tolerate process and voltage variations after four-point calibration is presented. Although four-point calibration is required in the proposed ATWS, it can overcome process and voltage variations and achieve a relatively small temperature as compared to current smart temperature sensors. In addition, the proposed ATWS is implemented with standard cells which makes it has best portability and is suitable for use as an on-chip temperature sensor for dynamic thermal management.

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