Yield Improvement in Memory Compiler Generated SRAM with Inter-Die Variations

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***Abstract*— As the technology scales down to nanometer, the yield degradation caused by inter-die variations is getting worse. Using adaptive body bias is an effective method to eliminate the yield degradation, however we need to know a die having high threshold voltage or low threshold voltage (also called process corner) in order to use this technique. Unfortunately, it is hard to detect the process corner when PMOS and NMOS variations are uncorrelated. In this paper, we propose some improved circuits of delay monitor and leakage monitor for both PMOS and NMOS, which are uncorrelated in inter-die variations. The experimental results show that our circuits can clearly distinguish each process corner of PMOS and NMOS, thus improve the yield obviously by adopting correct body bias.**

I. Introduction

With reduction in technology feature sizes, the MOS size becomes very small. The threshold voltage variations caused by random dopant fluctuation (RDF) is inversely proportional to gate area [1], thereby the probability of device mismatch increases greatly. This is especially obvious to SRAM. Because SRAM cell always uses the smallest manufacture devices size [2] to ensure having high density, SRAM faces with more challenges about process variations than normal digital circuits.

In recent years, process variation becomes a very important issue. As the technology scales down to nanometer, the device parameters, such as gate length and oxide thickness, suffer from significant variations. In each kind of process variations, the threshold voltage mismatch is one of the most important issues. The situation happens when PMOS and NMOS variations are uncorrelated, it is hard to detect the process corner. The reason is that when detecting the process corner of PMOS, the results will be interfered from NMOS variations, which makes the detection fail. Hence we need an improved circuit to be able to detect PMOS and NMOS variations individually. If we do not consider the process variations in design stage, the real yield of the design will be far away from our expectation.

Memory is commonly used in various kinds of ICs. When designers design a digital circuit, memory compiler is a popular tool to provide the designers SRAM so as to integrate memory circuit with their digital circuits. In order to guarantee good yield, a memory compiler should be able to provide the components with the tolerance to high process variations. In this work, our purpose is to make the circuits generated from memory compiler better and immune from process variations. Our main contributions are as follows:

- We propose some improved circuits for delay monitor and leakage monitor to detect both PMOS and NMOS variations. Based on the detection results, we apply global body bias to both PMOS and NMOS. The goal is to mitigate the read-write fail caused by the inter-die variations.
- In order to have more complete analysis, we not only use single port SRAM but also use dual port SRAM as test circuits. In some cases PMOS variations have more influence on the predictive yield than NMOS variations, hence both NMOS and PMOS detect circuits are more effective to improve yield.
- The experimental results show that our yield improvement is much better than the improvement using only NMOS body bias in some variations situations, and our circuits can guarantee that we always apply correct PMOS body bias.

The rest of the paper is organized as follows. In Section II, we discuss how process variations decrease the yield and review some previous works about how to eliminate the effect of inter-die variations. In Section III, we present our improved circuits, and Section IV shows the experimental results. We conclude our work in Section V.

II. Preliminary

In this section, we introduce previous works in using adaptive body bias to decrease the effect of process variations.

A. Previous Works

In order to decrease the effect of process variations in SRAM architectures, many methods have been proposed. Some new SRAM cell architectures are presented [3] [4]. Moreover, typical 6-T SRAM cell architecture use additional circuits to enhance the yield, such as using adaptive body bias [5] [6] [7]. Because the memory compiler use typical 6-T SRAM cell, hence we focus on adaptive body bias. By the results of [5] we can see that adaptive body bias is an effective method to improve SRAM yield. In order to use the technique we need some circuits to detect the process corner. In [5] [6] [7], the authors use leakage monitor and delay monitor to detect the dies having high threshold voltage or low threshold voltage. In [8] the authors propose a method using delay and slew-rate monitor to detect the process corner.

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1) Adaptive Body Bias: The principle of adaptive body bias is that when we know that a die belongs to high threshold voltage, we can provide this die forward body bias to decrease the threshold voltage. Similarly, when we know that a die belongs to low threshold voltage, we can provide this die reverse body bias to increase the threshold voltage. Using this technique we can make every die tend to have normal threshold voltage, and improve the yield. This method is used to improve the yield of logic design [9]. The authors of [5] use this method to improve SRAM yield for the first time.

2) Leakage Monitor: Here we describe the principle of leakage monitor. In Fig. 1 we can see the authors use a current sensor circuit to monitor the leakage of SRAM array and generate a voltage to comparator. Then the comparator circuits compare this voltage with two reference voltages. These two reference voltages represent a die at high threshold corner and low threshold corner respectively. According to this result, we can make sure that this die belongs to high or low threshold, and the body bias selection circuit will apply correct body bias to the SRAM array. Besides, a large PMOS switch bypasses the leakage monitor at normal mode operation.

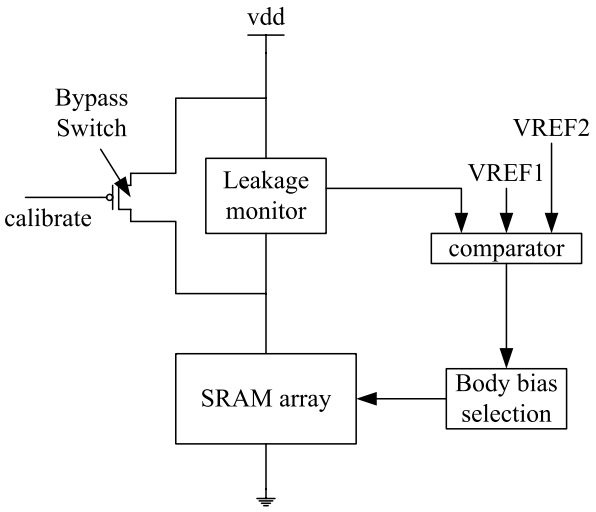

Fig. 1. The leakage monitor approach to detecting inter-die variations [6].

3) Delay Monitor: Another way to know a die with high or low threshold voltage is using delay monitor[6] [7]. Fig. 2 shows the delay monitor circuits. It is composed of a 600 stages long inverter chain, a counter circuit, and the comparator circuits. We introduce the principles of delay monitor as follows. First, a calibrate signal passes through the long inverter chain and enables the counter at the same time. Second, the counter is disabled when calibrate signal comes out the inverter chain. Finally, the comparator circuits are used to compare with two references which are represented as low threshold corner and high threshold corner. The body bias selection circuits will apply the right body bias to SRAM array according to the result of comparator.

B. Problem Description

In real manufacturing flow, the lithography parameters cause the PMOS and NMOS having correlated inter-die shift. It means that both PMOS and NMOS move to high or low threshold voltage. Other sources, such as global variations of doping density may cause non-correlated threshold voltage shift [7]. So it is necessary to detect the process corner of PMOS and NMOS variations individually. Since previous works ([5] [6] [7]) assumed that PMOS and NMOS variations are correlated, which is not complete correct, we try to develop different circuits to detect the variations of PMOS and NMOS individually.

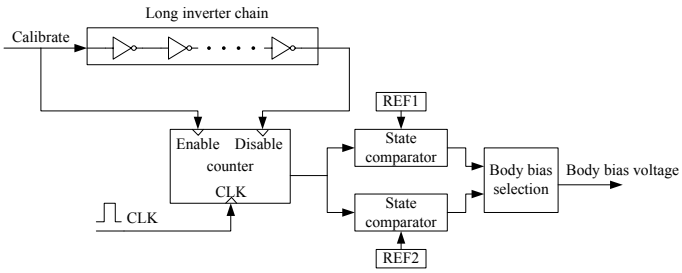

Fig. 2. The delay monitor approach to detecting inter-die variations [6].

III. Improved Circuits for PMOS and NMOS Variations

In this section we first present the results of using the circuits in [6] to detect the process corner when PMOS and NMOS variations are uncorrelated. Then we discuss our improved circuits of leakage monitor and delay monitor to further distinguish those variations individually.

A. Delay Monitor for PMOS and NMOS Variations

Table I shows the variations results of the circuits discussed in [6], but the PMOS and NMOS variations are not always correlated. We assume that the die suffers from both inter-die and intra-die variations: the intra-die variations have 75mv at 3-sigma and the distribution is random (based on [10]), the inter-die variations are given from 125mv to 175mv.

TABLE I
The required clock cycles at different inter-die variations using the circuit in [6].

125-125	PMOS / NMOS	HVT	NVT	LVT
	HVT	15	13	♣11
	NVT	♠13	11	◇9
	LVT	♣11	9	8
150-150	PMOS / NMOS	HVT	NVT	LVT
	HVT	17	13	♣11
	NVT	14	11	◇9
	LVT	♣12	9	8
175-175	PMOS / NMOS	HVT	NVT	LVT
	HVT	18	14	♣11
	NVT	♠15	11	◇9
	LVT	♣12	9	8

In Table I, the first column shows the inter-die variations of PMOS and NMOS. Other columns with HVT, NVT, LVT

represent high threshold voltage, normal threshold voltage, and low threshold voltage respectively. The numerical values in the last 3 columns express the required clock numbers.

Based on [6], we may set the high threshold corner at 13 cycles and the low threshold corner at 10 cycles. We observe that when PMOS has high threshold voltage and NMOS has low threshold voltage (or PMOS has low threshold voltage and NMOS has high threshold voltage), the traditional delay monitor will be under the impression that this die has normal threshold voltage and suggest the NMOS zero body bias. We indicate this situation with symbol ♣ in Table I. Another error will happen when PMOS has high threshold voltage and NMOS has normal threshold voltage. In this case, the circuits will be under the impression that the NMOS has high threshold voltage and suggest NMOS forward body bias, in result we get the wrong body bias. This situation is indicated with symbol ♠. The last kind of error happens when PMOS has low threshold voltage and NMOS has normal threshold voltage. In this case the circuits will be under the impression that the NMOS has low threshold voltage and suggest the reverse body bias. We indicate this situation with symbol ♢.

Based on the previous discussion, we know that if we do not concern the PMOS variations, using delay monitor may make a mistake and the probability of making this mistake is nearly 50%. Moreover, it may cause the yield worse than without using body bias in some cases. Therefore, it is necessary to concern the effect of both PMOS and NMOS variations.

1) PMOS Variations Detector Using Delay Monitor: By observing Table I, we can see that if we know the process corner of PMOS, then we can detect the process corner of NMOS successfully. For example, if we know that PMOS has high threshold voltage, the delay at 125mv assumption for inter-die variations will be 11 or 13 or 15 cycles. These three kinds of values are divided away hence we can distinguish each other and know the NMOS variations. Therefore the problem becomes to know the process corner of the first type MOS variations. Our approach is presented in the following subsections.

If we want to detect the process corner of PMOS, we must remove the effect of NMOS variations. In order to achieve this, we let the PMOS and NMOS mismatch, that is, the size of PMOS are 100nm/90nm and NMOS are 110nm/90nm. Here we let PMOS have less driver ability. The delay will be dominated by PMOS thus degrading the effect of NMOS. We do not use 1V supply voltage, but use 0.7V in order to increase the difference between PMOS and NMOS driver ability. Furthermore, we do not use the normal body bias, but apply forward body bias to NMOS, and apply reverse body bias to PMOS of detect circuit at detecting stage.

Table II shows the results when we use our circuits to detect PMOS inter-die variations. We set the PMOS high threshold corner at 17 and low threshold corner at 9. The results show that we can separate each kind of PMOS variations. Here 'OK' in Table II and following tables means the required cycle number is larger than 24.

2) NMOS Variations Detector Using Delay Monitor: Now we have already detected PMOS variations, the next stage is to detect the process corner of NMOS. In this stage, we can not change the size of inverters since the inverter size has been determined in previous stage. In previous section, we know that our MOS sizes are chosen for easily detecting PMOS variations. Here we want only NMOS variations to change delay time, we must correct the body bias of both PMOS and NMOS. We apply reverse body bias to NMOS and apply forward body bias to PMOS. The result shows in columns 3 to 5 in Table III. The result shows that our method has some effects but still not enough. The main problem is that the delay time is too short when PMOS has low threshold. In other words, PMOS variations still affect the delay time hence the detection of NMOS variations will fail. We need the following improved circuits to have better detections.

TABLE II

THE RESULTS OF DETECT PMOS INTER-DIE VARIATIONS. IN THIS TABLE WE CAN SEE THAT EACH KIND OF PMOS VARIATIONS(HVT NVT AND LVT) ARE SEPARATED.

125-125	PMOS NMOS	HVT	NVT	LVT
	HVT	OK	13	8
	NVT	17	10	6
	LVT	OK	9	5
150-150	PMOS NMOS	HVT	NVT	LVT
	HVT	OK	14	8
	NVT	21	10	6
	LVT	OK	9	5
175-175	PMOS NMOS	HVT	NVT	LVT
	HVT	OK	15	8
	NVT	OK	10	6
	LVT	OK	9	5

TABLE III

THE RESULTS OF DETECTING NMOS VARIATIONS.

125-125	PMOS NMOS	HVT	NVT	LVT		HVT	NVT	LVT
	HVT	15	15	11		15	16	16
	NVT	12	11	8		12	12	13
	LVT	10	9	6		10	10	11
150-150	PMOS NMOS	HVT	NVT	LVT		HVT	NVT	LVT
	HVT	18	16	11		18	17	16
	NVT	13	11	7		13	12	12
	LVT	10	9	6		10	10	11
175-175	PMOS NMOS	HVT	NVT	LVT		HVT	NVT	LVT
	HVT	20	16	10		20	17	15
	NVT	14	11	7		14	12	12
	LVT	11	8	5		11	9	10

3) Modified Circuits for NMOS Variations: In Table III columns 3 to 5 we can see that PMOS variations still affect the delay time. We do not separate each variation of NMOS, but we observe that if we change the initial value of counter (Fig. 2) the results will be different. In order to accomplish this, we delay the enable signal of the counter circuit and show the block diagram in Fig. 3.

If we have normal threshold PMOS, we let the enable signal delay 1 cycle to reach the counter circuit. If we have low

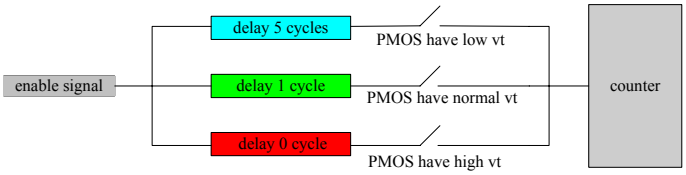

Fig. 3. Modified circuit block diagram for detecting NMOS variations. This circuit can eliminate the effect of PMOS variations when detecting the process corner of NMOS.

threshold PMOS, we will delay 5 cycles. The modified results are shown in Table III columns 7 to 9. Now we can know the process corner of NMOS by detecting the delay time. If the delay is more than 15 cycles, the NMOS belongs to high threshold NMOS. Similarly if the delay time is less than 11 cycles, the NMOS belongs to low threshold NMOS and others belong to normal threshold NMOS.

In summary, our circuits have some difference with the traditional delay monitor. First, we make the inverter MOS mismatch to let the PMOS dominate the delay time. Second, we apply body bias for detect circuit at detecting stage to make the detection successfully. Third, we add a delay switch circuits to remove PMOS variations when NMOS variations are detected.

B. Leakage Monitor for PMOS and NMOS Variations

Similar to delay monitor, if we use traditional circuits to detect the variations without thinking PMOS variations, the errors will occur. The following subsections will present our modified leakage monitor circuits.

1) Inverter Array: Here we do some modification to the architecture Fig. 1 for our usage. We replace leakage source from the SRAM array to an inverter array. The reasons are as follows. First, we use inverter array to be the test circuit, then bypass PMOS is no longer needed. Second, we can give a value we need but not limit on 0V or 1V to the input signal of inverter. We also change the loading circuits of current mirror since we want our modified circuits be able to detect NMOS and PMOS individually. Finally, we will add body bias on current mirror circuits when we detect NMOS variations.

2) PMOS Variations Detector Using Leakage Monitor: Similar to delay monitor, we detect the PMOS variations first. We modify the loading of the current mirror. The circuits are shown in Fig. 4(a). We cascade three NMOS devices and connect their gate with a metal line to make them have the same gate voltage. The output is taken out by net1, and the result is shown in Table V. The numerical values in the last 3 columns express the output voltage of current mirror. We can see that cascade three NMOSs remove the effect of active load NMOS variations.

3) NMOS Variations Detector Using Leakage Monitor: In previous stage we have already known the process corner of PMOS, and we need to detect the NMOS variations. Here we only use normal current mirror. In order to remove the influence of PMOS (two PMOS current mirror driver, MP1 and MP2), we give adaptive body bias to PMOS driver based on the results of first stage. The circuits show in Fig. 4(b), and the result is shown in Table VI.

TABLE IV

THE RESULTS OF USING TRADITIONAL ACTIVE LOAD TO DETECT THE PROCESS CORNER OF PMOS.

PMOS-NMOS	PMOS / NMOS	HVT	NVT	LVT
125-125	HVT	0.5456	0.7190	0.8411
	NVT	0.4399	0.5991	0.7126
	LVT	0.3219	0.4793	0.5944

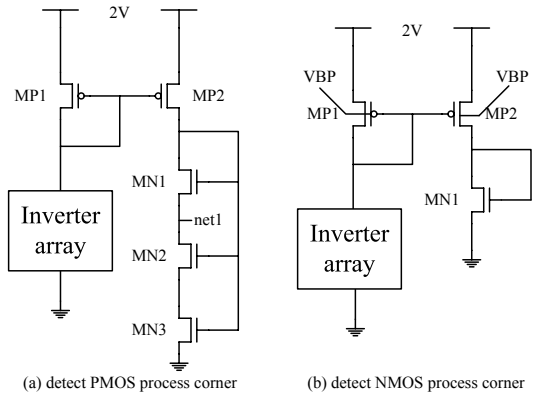

Fig. 4. (a)We replace the active NMOS loading with cascade three NMOS devices when detecting PMOS variations.(b)We apply body bias to the two PMOS driver when detecting the process corner of NMOS.

C. Discussion

When using our delay monitor circuits, the reason of detecting PMOS variations first is that its size is smaller than the circuit of detecting NMOS variations coming first. If we detect NMOS variations first, the NMOS variations must dominate the delay, in other words, the PMOS size must be much larger than NMOS. The required size may be PMOS with 400nm/90 and NMOS with 100nm/90nm to make PMOS have twice driving force to NMOS. The area is almost 2.5 times larger than the circuit which detecting PMOS variations first.

TABLE V

THE RESULTS OF MODIFIED CIRCUITS DETECT PMOS VARIATIONS.

125-125	PMOS / NMOS	HVT	NVT	LVT
	HVT	0.2107	0.426	0.532
	NVT	0.2258	0.4196	0.5261
	LVT	0.2177	0.4022	0.5126
125-200	PMOS / NMOS	HVT	NVT	LVT
	HVT	0.2215	0.4281	0.5352
	NVT	0.2258	0.4196	0.5261
	LVT	0.214	0.3933	0.5040
200-125	PMOS / NMOS	HVT	NVT	LVT
	HVT	0.1367	0.4265	0.5631
	NVT	0.1458	0.4196	0.5586
	LVT	0.1367	0.4022	0.5457

TABLE VI

THE RESULTS OF OUR CIRCUITS TO DETECT NMOS VARIATIONS.

125-125	PMOS / NMOS	HVT	NVT	LVT
	HVT	0.5336	0.4530	0.4820
	NVT	0.4160	0.3316	0.36
	LVT	0.2892	0.2154	0.2440
125-200	PMOS / NMOS	HVT	NVT	LVT
	HVT	0.6142	0.5314	0.5608
	NVT	0.4160	0.3316	0.36
	LVT	0.2303	0.1465	0.1752
200-125	PMOS / NMOS	HVT	NVT	LVT
	HVT	0.4916	0.4530	0.5271
	NVT	0.3742	0.3316	0.4032
	LVT	0.2576	0.2154	0.2865

IV. EXPERIMENTAL RESULTS

We implement our circuits in HSPICE, and use memory compiler from FARADAY to build single port SRAM and dual port SRAM as our test circuits. We use the UMC 90nm CMOS library to implement our circuits.

A. Single Port SRAM

We use memory compiler to compile a 64-word (each word has 32 bits) single port SRAM. We use Monte-Carlo method to test the failure probability. We choose 640 cells per circuit as our test samples, and the result is shown in Table VII to Table IX.

In Table VII, each test circuit suffers from both inter-die and intra-die variations. The value of inter-die variations is 125mv and the value of intra-die variations is 75mv. The meaning of each element is as follows. The first column represents the process corner of PMOS and NMOS respectively. The second column represents the original circuits without using body bias. The sub-columns 0 and 1 represent the action of 'write 0 then read the data out' and 'write 1 then read it out' respectively. Other numerical values represent the failure numbers in 640 times test. The third column represents that we only use NMOS body bias and we assume that all predictions are correct. The fourth column presents the result of using the circuits in [6]. And the final column represents the results of using our circuits. We can see that our improved circuits will always get the right prediction, and our yield improvement will be better than the technique applying only NMOS body bias.

In Table VIII, all experimental setups are the same as in Table VII except for the 150mv assumption for inter-die variations. We can see that when PMOS and NMOS both have high threshold the yield degrades very much, and using only NMOS body bias can not satisfy the requirement of yield improvement. The yield improvement of using both PMOS and NMOS body bias is obviously.

In Table IX, all experimental setups are the same as in Table VII except for the 175mv assumption for inter-die variations. Here we notice that our circuits will no longer always get the right predictions. When PMOS have high threshold and NMOS have normal or low threshold, our circuits will get the right process corner of PMOS but get the wrong prediction of NMOS. Even we get the wrong predictions, our yield are still very close to the right prediction of only use NMOS body bias.

TABLE VII

TOTAL FAILURE NUMBER OF THE SINGLE PORT SRAM WITH 125MV ASSUMPTION FOR INTER-DIE VARIATIONS AND 75MV ASSUMPTION FOR INTRA-DIE VARIATIONS.

125mv	Without body bias		Only NMOS body bias		[6]		Ours	
PMOS-NMOS	0	1	0	1	0	1	0	1
high– high	25	108	2	1	2	1	2	0
high– zero	3	0	3	0	4	0	0	0
high– low	14	9	9	0	14	9	6	0
zero– high	0	0	0	0	0	0	0	0
zero– low	4	0	0	0	0	0	0	0
low – high	0	0	0	0	0	0	0	0
low – zero	0	0	0	0	0	0	0	0
low – low	0	0	0	0	0	0	0	0

TABLE VIII

TOTAL FAILURE NUMBER OF THE SINGLE PORT SRAM WITH 150MV ASSUMPTION FOR INTER-DIE VARIATIONS AND 75MV ASSUMPTION FOR INTRA-DIE VARIATIONS.

150mv	Without body bias		Only NMOS body bias		[6]		Ours	
PMOS-NMOS	0	1	0	1	0	1	0	1
high– high	45	508	38	432	38	432	31	97
high– zero	7	0	7	0	13	0	1	0
high– low	24	28	19	10	24	28	14	5
zero– high	0	0	0	0	0	0	0	0
zero– low	6	1	2	0	2	0	2	0
low – high	0	0	0	0	0	0	0	0
low – zero	0	0	0	0	0	0	0	0
low – low	4	0	2	0	2	0	4	0

B. Dual Port SRAM

Similar to single port SRAM, we use memory compiler to build a 64-words (each word has 32 bits) dual port SRAM in our test circuits. The dual port SRAM has two ports: port A and port B. We use port A to write the data to SRAM cell and use port B to read out the stored data. We use Monte-Carlo method to test the failure probability. We choose 640 cells per circuit as our test samples, and the result shows in Table X and Table XI. The means of each element are the same as Table VII and Table VIII.

In Table X we can see a huge difference to single port SRAM. When both PMOS and NMOS have high threshold voltage, we get the results of 640 failures in read 1. This means that the failure probability is 100%, and the failure is caused by the unsuccessful writing 1 to SRAM cell, hence we always get the 0 at output signal. This problem almost can not be solved by using only NMOS body bias. On the other hand, using both PMOS and NMOS body bias can solve the problem very well.

In Table XI, we see that our circuits can not solve the all

TABLE IX

TOTAL FAILURE NUMBER OF THE SINGLE PORT SRAM WITH 175MV ASSUMPTION FOR INTER-DIE VARIATIONS AND 75MV ASSUMPTION FOR INTRA-DIE VARIATIONS.

175mv	Without body bias		Only NMOS body bias		[6]		Ours	
PMOS-NMOS	0	1	0	1	0	1	0	1
high– high	74	522	70	501	70	501	49	162
high– zero	17	0	17	0	34	0	15	0
high– low	34	35	27	30	34	35	28	32
zero– high	0	0	0	0	0	0	0	0
zero– low	16	5	8	1	8	1	8	1
low – high	0	0	0	0	0	0	0	0
low – zero	0	0	0	0	0	0	0	0
low – low	31	0	19	0	19	0	15	0

TABLE X

TOTAL FAILURE NUMBER OF THE DUAL PORT SRAM WITH 125MV ASSUMPTION FOR INTER-DIE VARIATIONS AND 75MV ASSUMPTION FOR INTRA-DIE VARIATIONS.

125mv	Without body bias		Only NMOS body bias		[6]		Ours	
PMOS-NMOS	0	1	0	1	0	1	0	1
high– high	0	640	16	598	16	598	3	12
high– zero	0	1	0	0	0	0	0	0
high– low	2	0	2	0	2	0	2	0
zero– high	0	0	0	0	0	0	0	0
zero– low	0	0	0	0	0	0	0	0
low – high	1	5	0	0	1	5	0	0
low – zero	0	0	0	0	0	0	0	0
low – low	0	0	0	0	0	0	0	0

failure problem happened at both PMOS and NMOS having high threshold voltage. We find that the corner point of all failure happened is when both PMOS and NMOS having 115mv inter-die voltage higher than normal threshold, and we use adaptive body bias can not fix so much inter-die variations.

V. CONCLUSION

In this work, we have proposed some improved circuits of delay monitor and leakage monitor. These circuits can correctly detect both PMOS and NMOS variations, and improve the yield by decreasing the influence of inter-die variations. All of our test circuits are built by a widely used memory compiler. The experimental results show that some situations can not improve yield by using only NMOS body bias, but using both PMOS and NMOS body bias can improve significantly. Besides, the results also show that our proposed circuits can almost get the right predictions of variations. Even we get wrong prediction of NMOS, our yield can still improve by adapting correct PMOS body bias. We conclude that our yield is always better than only using NMOS body bias circuits.

TABLE XI

TOTAL FAILURE NUMBER OF THE DUAL PORT SRAM WITH 150MV ASSUMPTION FOR INTER-DIE VARIATIONS AND 75MV ASSUMPTION FOR INTRA-DIE VARIATIONS.

150mv	Without body bias		Only NMOS body bias		[6]		Ours	
PMOS-NMOS	0	1	0	1	0	1	0	1
high– high	0	640	0	640	0	640	0	640
high– zero	3	35	3	35	5	62	0	0
high– low	7	8	6	6	7	8	2	0
zero– high	13	0	5	0	5	0	5	0
zero– low	6	0	4	0	4	0	4	0
low – high	6	19	2	7	6	19	1	3
low – zero	0	8	0	8	0	10	0	0
low – low	8	8	4	5	4	5	3	0

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