This full text paper was peer-reviewed at the direction of IEEE Instrumentation and Measurement Society prior to the acceptance and publication.

An All-Digital Voltage Sensor for Static Voltage Drop Measurements

Ching-Che Chung, *Member IEEE*, and Mei-I Sun
Department of Computer Science and Information Engineering
National Chung Cheng University
No. 168 University Rd., Min-Hsiung, Chia-Yi, Taiwan
Email:wildwolf@cs.ccu.edu.tw

***Abstract*—One of the main challenges in semiconductor industry is the variability in devices and circuit parameters which will harm the performance and the energy efficiency of the circuit. In addition, voltage fluctuation also makes the performance of the design unpredictable. Due to the high level integration of the system-on-a-chip (SoC), it becomes more and more important to monitor the IR drop of the power network during chip operation. The proposed all-digital on-chip voltage sensor which uses a relative reference modeling (RRM) is presented. After one-point calibration at 1.1V, the proposed all-digital voltage sensor can monitor the operating voltage of the chip and outputs digital codes for SoC chip debugging and testing. It has a maximum error 16.4mV with process, voltage, and temperature (PVT) variations.**

Keywords— On-chip monitoring; IR-drop; Voltage sensor; Process and Temperature Calibration

I. INTRODUCTION

Nowadays, the high level integration of the system-on-a-chip (SoC) causes that the voltage transients (IR drop) issue of the power network becomes more serious and unpredictable. IR drop may lead to unexpected performance degradation to the chip. As a result, on-chip voltage sensors which are placed in different locations of the SoC can provide useful diagnosis information to the chip designer for chip debugging and testing. Most of the current on-chip voltage sensors [1],[3] require the calibration process to map the measured analog voltage values into digital codes. However, the process, voltage, and temperature (PVT) variations affect the relationship between the measured voltage values and the output digital codes. Thus, the voltage sensor [1] needs to execute the calibration process periodically (e.g. every 1ms) for compensation for temperature variations. In addition, in each calibration process, it also requires three input reference voltages (0.8V, 0.9V, and 1.0V) for 2nd-order polynomial regression which makes the voltage sensor [1] not easily applicable for SoC design.

The voltage sensor [3] also requires three different input reference voltages for sensor calibration. Each on-chip voltage sensors are calibrated individually, and the process variation of the voltage sensor is normalized after calibration. However, the error of the voltage sensor (i.e. difference between the sensor output voltage and the actual voltage of the measured node) will be increased accordingly with temperature variations after chip calibration since the calibration for each voltage sensor is performed once. The voltage sensor [2] requires adjusting the input voltage of the controllable delay block of the voltage sensor with PVT variations. However, when the operating conditions are changed, this calibration process for the proposed sensor needs to be performed again. Or the operation of the voltage sensor may be not worked correctly.

In this paper, an all-digital voltage sensor which uses a relative reference modeling (RRM) is presented. After one-point calibration at 1.1V, the proposed all-digital voltage sensor can determine the process variation of the voltage sensor and compensates for the process variations. After that, the proposed temperature sensor can measure the temperature variations and compensates for the temperature variations. Finally, the linear calculator of the proposed all-digital sensor converts the measured voltage values to digital codes. The proposed all-digital voltage sensor has a maximum error 16.4mV with PVT variations after one-point calibration.

The rest of this paper is organized as follows: Section II describes the architecture of the proposed all-digital voltage sensor. Section III shows the characteristics of the proposed delay ratio estimator (DRE). Section IV shows the experimental results of the proposed all-digital voltage sensor. Finally, Section V concludes with a summary.

II. PROPOSED ALL-DIGITAL VOLTAGE SENSOR

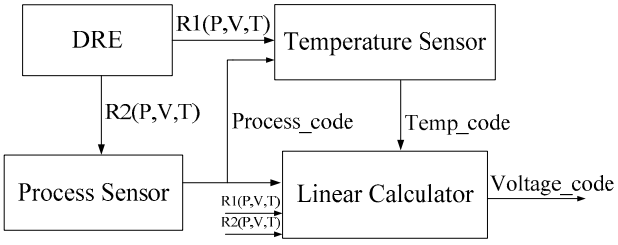

Fig. 1. Proposed all-digital voltage sensor.

The architecture of the proposed all-digital voltage sensor is shown in Fig. 1. The proposed all-digital voltage sensor consists of a delay ratio estimator (DRE), a process sensor, a

This work was supported in part by the Ministry of Science and Technology of Taiwan, under Grant MOST-103-2221-E-194-063-MY3.

978-1-4799-7250-0/16/$31.00 ©2016 IEEE

temperature sensor, and a linear calculator. The delay ratio estimator shown in Fig. 2 consists of three ring oscillators which were made of different delay cells: reference delay cell (RDC), compared delay cell 1 (CDC1), and compared delay cell 2 (CDC2). The delay ratio is the ratio of the propagation delay time between two delay cells and was defined in [4]. The delay ratio is a function of process, voltage, and temperature conditions. The DRE can compute the delay ratios among three delay cells with PVT variations and outputs as R1(P,V,T) and R2(P,V,T), respectively.

$$R1(P,V,T) = \frac{CRO1_{CNT}}{RRO_{CNT}}, \quad R2(P,V,T) = \frac{CRO2_{CNT}}{RRO_{CNT}} \quad (1)$$

As shown in Fig. 2, in the proposed DRE, the outputs of the ring oscillators are connected to three counters. The counters record the oscillation cycles of the ring oscillators. When the output of the RRO counter is counted from 0 to N_{TIME}, three counters are all stopped. Then the counter values can be used to compute the delay ratios R1(P,V,T) and R2(P,V,T) as illustrated in Eq. 1. After that, these counters are reset and restarted again. Therefore, the DRE will keep computing the delay ratios when voltage and temperature conditions are changed during chip operation. In the proposed DRE, N_{TIME} is set to 1023, and thus, RRO_{CNT} is equal to $1024=2^{10}$. Thus, in Eq. 1 we don't need to use dividers when computing the delay ratios. The period of RRO ring oscillator is 8.6ns, and thus, the proposed DRE takes 8.8µs to compute the delay ratios which also limits the highest sampling rate of the proposed all-digital voltage sensor.

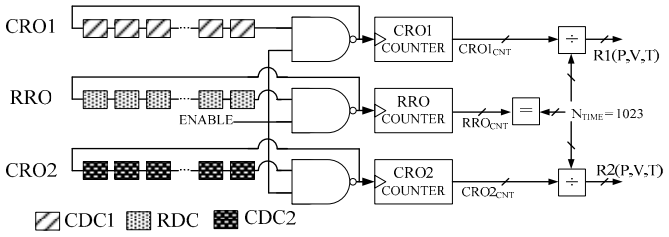

Fig. 2. Proposed delay ratio estimator.

As shown in Fig. 1, the DRE outputs delay ratios to the process sensor and the temperature sensor. The proposed process sensor uses the delay ratios to determine the process variations of the chip and outputs the process code to the temperature sensor and the linear calculator. The proposed temperature sensor uses the delay ratios and process code to calculate the operating temperature of the chip and outputs the temperature code to the linear calculator. Finally, the proposed linear calculator uses the delay ratios, process code, and temperature code to compute the operating voltage of the chip and outputs digital codes (voltage_code).

The proposed all-digital voltage sensor for static voltage drop monitoring adopts a relative reference modeling (RRM) in circuit design. The similar relative reference modeling concept is also used in [5] to adjust the frequency control word of the all-digital phase-locked loop (ADPLL) and compensates for temperature variations. The propagation delay time of logic cells are easily affected by PVT variations. Our goal is to eliminate the PVT variations from the proposed all-digital voltage sensor to make it reliable and stable under the operating range. The propagation delay time of different delay cells have different voltage and temperature variations dependence. As a result, we can choose suitable delay cells from the cell-library to build up the DRE to obtain the required delay ratio characteristics over PVT variations. Then the proposed process sensor and temperature sensor can use the delay ratios to determine the process and temperature variations. As a result, the relationship between the absolute voltage value and digital codes can be kept over PVT variations. In addition, the proposed all-digital voltage sensor only requires one-point calibration at 1.1V, and the operating chip temperature will not affect the calibration process. Therefore, a temperature chamber is not necessary for the proposed all-digital voltage sensor, and then, the calibration cost can be greatly reduced in mass production.

III. Characteristics of the DRE

The proposed all-digital voltage sensor is implemented in TSMC 90nm CMOS process with standard cells. We need to perform many SPICE circuit simulations of the DRE to obtain the delay ratios with PVT conditions. In addition, we can change the delay cells in the DRE to obtain the desired delay ratio characteristics. Fig. 3 shows the simulated R2(P,V,T) curves, where TT means typical process corner, FF means best process corner, and SS means worst process corner in the SPICE model. The desired R2(P,V,T) characteristic is that the values of R2(P,V,T) at 1.1V are not overlapped in different process corners. Therefore, the simulated values of R2(P, V, T) can be used to identify the process variations of the voltage sensor when the process variation is unknown. Moreover, the simulated threshold values to determine the process corner are stored in the process sensor shown in Fig. 1. Then, after chip fabrication, if we calibrate the chip at 1.1V, and the output R2(P, V, T)*1024 of the DRE is 640. The value of R2(P, V, T) is close to the simulated SS process corner at 1.1V. Therefore, the proposed process sensor can determine that the fabricated voltage sensor is at SS process corner without temperature information.

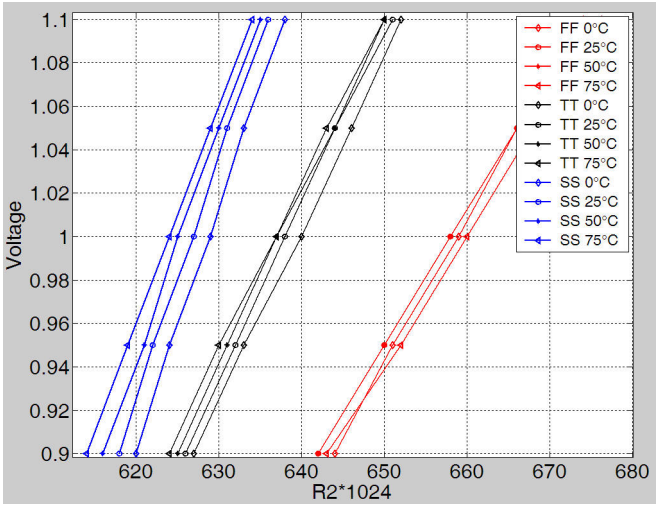

Fig. 3. Simulated R2(P, V, T) curves.

Fig. 4 shows the simulated R1(P,V,T) curves. The desired R1(P,V,T) characteristic is that at each process corner (TT, SS, FF), the values of R1(P,V,T) at different temperature are not overlapped. Therefore, the simulated values of R1(P, V, T) can be used to identify the temperature variations of the voltage sensor when the temperature variation is unknown. Moreover, the simulated threshold values to determine the temperature value are stored in the temperature sensor shown in Fig. 1. Then, after chip was calibrated at 1.1V, if the process corner is known as SS process corner by the process sensor, and the output R1(P, V, T)*1024 of the DRE is 1040. Then, the value of R1(P, V, T) is close to the simulated condition at 50°C in SS process corner. Therefore, the proposed temperature sensor can determine that the chip temperature of the voltage sensor is at 50°C.

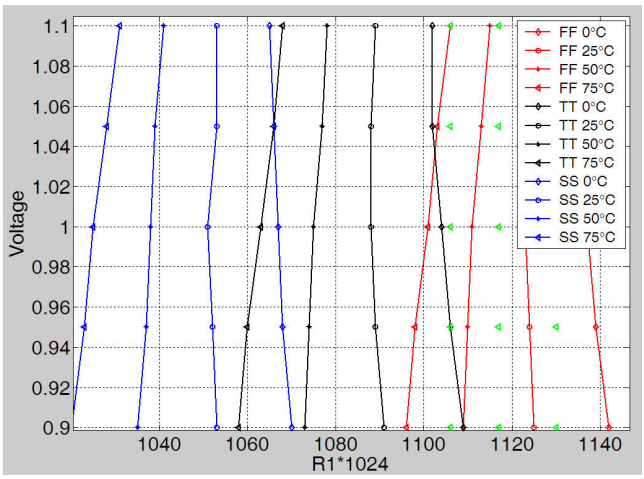

Fig. 4. Simulated R1(P, V, T) curves.

In the proposed all-digital voltage sensor, the relationship between the measured voltage values and the output digital codes are fixed even with PVT variations. The output voltage value is the voltage_code divided by 2^{15}. For example, if the output voltage_code of the proposed all-digital sensor is 29,456, and then, the output voltage value is $29{,}456/2^{15} = 0.898$V. Fig. 5 shows the simulated (R1 - R2)/R1 curves. In each process corner, at different temperature, the relationship between (R1 - R2)/R1 and the measured voltage value (i.e. voltage_code) can be approximated as a linear equation, as expressed in Eq. 2. Therefore, the simulated values of (R1 - R2)/R1 can be used to determine slope and intercept of the linear equations to compute the output voltage_code. The simulated slope and intercept values are stored in the linear calculator. After chip fabrication, if the process corner is known as SS process corner by the process sensor, and the voltage sensor is at 50°C by the temperature sensor. Then, the proposed linear calculator can use the suitable linear equation from the simulation results to compute the output voltage_code with the current value of (R1 - R2)/R1.

$$voltage\_code = 2^{15} \times \left(slope \times \frac{R1 - R2}{R1} + intercept \right) \quad (2)$$

After chip fabrication, the proposed all-digital voltage sensor needs to be calibrated at 1.1V. During the calibration process, the chip operating temperature is not important, since the proposed process sensor can determine the process corner of the voltage sensor without temperature information as illustrated in Fig. 3. Therefore, a temperature chamber is not necessary for the proposed all-digital voltage sensor, and then, the calibration cost can be greatly reduced in mass production. When the process_code is determined, the proposed temperature sensor can determine the chip temperature (temp_code) when the operating voltage ranges within 0.9V to 1.1V as illustrated in Fig. 4. Subsequently, the linear calculator of the proposed all-digital voltage sensor will use the value (R1 - R2)/R1 and selects a suitable linear equation to compute the measured voltage value (voltage_code) as illustrated in Fig. 5.

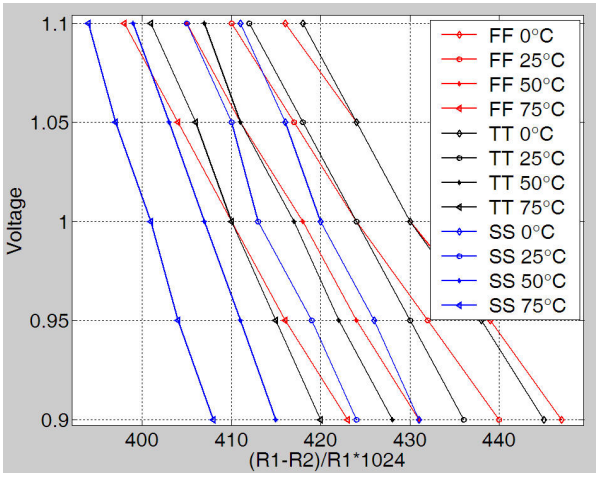

Fig. 5. Simulated (R1 - R2)/R1*1024 curves.

The detail operation flow of the proposed all-digital voltage sensor is shown in Fig. 6. The first step is to input the external parameters obtained from the simulation results (i.e. threshold values) for process sensor and temperature sensor, meanwhile the DRE starts to calculate the delay ratios. After DRE calculating R1(P,V,T) and R2(P,V,T), the process sensor can determine the process corner of the chip using R2(P,V,T). At chip run time, the temperature sensor uses R1(P,V,T) to determine the current working chip temperature. Then, the proposed linear calculator can calculate the current voltage. Finally, the circuit will start another cycle when operating voltage and temperature conditions are changed.

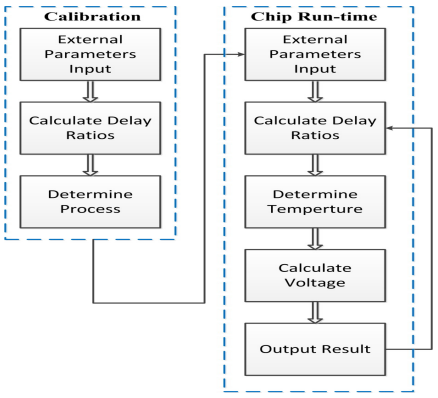

Fig. 6. Operation flow of the proposed all-digital voltage sensor.

IV. Experimental Results

The proposed all-digital voltage sensor is implemented in TSMC 90nm CMOS process with standard cells. The operating voltage ranges from 0.9V to 1.1V, and temperature range is from 0°C to 75°C. Fig. 7 shows the layout of the all-digital voltage sensor. We use the automatic placement and routing (APR) tools to design the chip. The active area of the test chip is 0.063 mm^2. The power consumption of the proposed design is 1.0068mW at 1.0V.

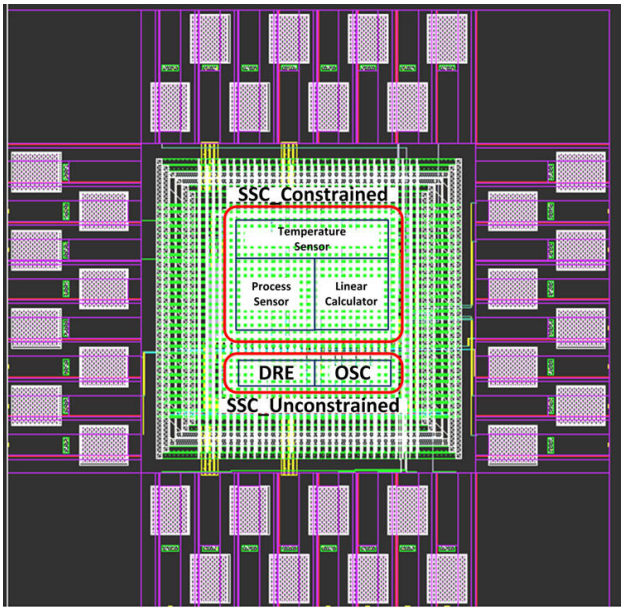

Fig. 7. Layout of the proposed all-digital voltage sensor.

We perform post-layout SPICE simulation of the proposed all-digital voltage sensor with different operating supply voltage. Fig. 8 shows the voltage error versus the input operating voltage for the proposed all-digital sensor with PVT variations. Voltage error means the difference between the sensor output voltage and the input operating voltage. The average voltage error is 5.1mV, and the maximum voltage error is 16.4mV with PVT variations. As compared to the voltage sensor [1], although the voltage sensor [1] has a maximum voltage error 4.81mV, it needs to execute the calibration process periodically (e.g. every 1ms) for compensation for temperature variations. In addition, in each calibration process, it also requires three input reference voltages (0.8V, 0.9V, and 1.0V) for 2nd-order polynomial regression which makes the voltage sensor [1] not easily applicable for SoC design. In the proposed all-digital sensor, the temperature sensor will keep monitoring the chip temperature, and the proposed linear calculator can use the suitable linear equation (with different slope and intercept) to compute the output voltage. As compared to the voltage sensor [3], it also requires three different input reference voltages for sensor calibration and temperature variations are not considered in [3]. The proposed all-digital sensor only requires one-point calibration at 1.1V, and a temperature chamber is not necessary for calibration process. As a result, the calibration cost of the proposed all-digital voltage sensor can be greatly reduced in mass production.

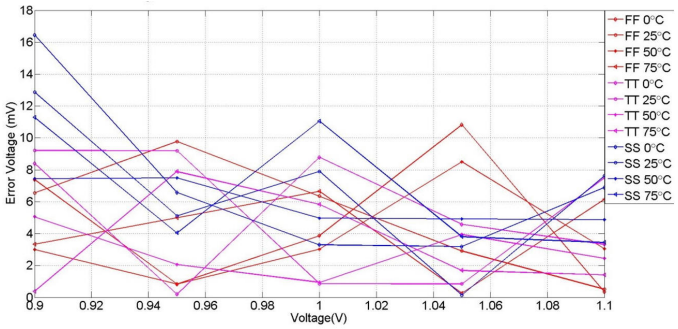

Fig. 8. Voltage error of the proposed all-digital voltage sensor vs. input voltage.

V. Conclusion

This work uses a relative reference modeling (RRM) to build up a delay ratio estimator (DRE). Then, the designed characteristics of the delay ratios by choosing suitable delay cells from the TSMC 90nm cell-library can be used to identify the process and temperature variations of the proposed all-digital voltage sensor. After one-point calibration at 1.1V, the linear calculator of the proposed all-digital voltage sensor can output an accurate voltage value with PVT variations. The proposed all-digital voltage sensor is implemented with standard cells which can reduce the design time and complexity for on-chip voltage sensor design, and is suitable for system-on-a-chip (SoC) applications.

Acknowledgment

The authors would like to thank their colleagues in the Silicon Sensor and System (S3) Laboratory of National Chung Cheng University for many fruitful discussions. The EDA tools supported by National Chip Implementation Center (CIC) are acknowledged as well.

References

[1] Chen-Hsiang Hsu, Shi-Yu Huang, Ding-Ming Kwai, and Yung-Fa Chou, "Worst-case IR-drop monitoring with 1GHz sampling rate," *in Proc. International Symposium on VLSI Design, Automation, and Test (VLSI-DAT)*, Apr. 2013.

[2] Hung Viet Nguyen and Youngmin Kim, "32nm FinFET-based 0.7-to-1.1V digital voltage sensor with 50mV resolution," *in Proc. International Conference on IC Design and Technology (ICICDT)*, May 2012.

[3] Rex Petersen, Pankaj Pant, Pablo Lopea, Aaron Barton, Jim Ignowski, and Doug Josephson, "Voltage transient detection and induction for debug and test," *in Proc. International Test Conference (ITC)*, Nov. 2009, pp. 1-10.

[4] Chien-Ying Yu, Jui-Yuan Yu, and Chen-Yi Lee, "A low voltage all-digital on-chip oscillator using relative reference modeling," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 20, no. 9, pp. 1615-1620, Sep. 2012.

[5] Yuji Satoh, Hiroyuki Kobayashi, Takeshi Miyaba, and Shouhei Kousai, "A 2.9mW, +/- 85ppm accuracy reference clock generator based on RC oscillator with on-chip temperature calibration," *in Proc. Symposium on VLSI Circuits*, Jun. 2014, pp. 1-2.