Power Reduction with Dynamic Sampling and All-Digital I/Q-Mismatch Calibration for A MB-OFDM UWB Baseband Transceiver*

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Abstract

A dynamic sampling and digital I/Q-mismatch calibration (IQM) in a MB-OFDM UWB baseband transceiver are proposed to reduce ADC power and analog IQM-calibration power. Measured transceiver power consumes 31.2mW, saving at least 43% ADC power and tolerating 10x IQM (2dB gain and 20 degree phase errors) of existing designs to reduce the power and design efforts from analog calibration circuits.

Keywords: dynamic sampling, I/Q mismatch, OFDM.

1. Introduction

In an ultra wideband (UWB) system, I/Q mismatch (IQM) from RF circuits degrades system packet error rate (PER) performance, and ADC circuit consumes about 50% analog front-end power (ADC×2+RF) [4][5]. To reduce power consumption while maintaining the same system performance, a multi-band OFDM (MB-OFDM) UWB baseband transceiver with dynamic sampling timing controller (DSTC) and digital IQM calibration is proposed here, saving ADC operation power and analog IQM-calibration circuit power, respectively.

A crucial power limitation 205mW is defined for MB-OFDM UWB system [1]. This constraint includes the power from a baseband processor, a pair of ADC circuits, and RF front-end circuits. For state-of-the-art ADC circuits, some representative designs are summarized in Fig. 1. It is found that no ADC circuits are qualified in the use of operating at sampling frequency higher than Nyquist rate (1056MS/s) while consuming circuit power within the constraint level (205mW) when a pair of ADCs (I and Q paths) are considered. In existing wireless transceiver design methodologies, however, ADC sampling frequency is over-sampled by a factor of 2x~9x [6]. To meet the power dissipation requirement, a DSTC is proposed with the aid of a phase-tunable clock generator (PTCG) to reduce the sampling frequency to Baud rate, i.e. 1x symbol rate, resulting in 70mW×2 ADC power saving [5] with only 1.9mW DSTC power overhead.

With the shrinking power of digital circuits, a digital IQM compensation circuit is proposed to migrate the analog calibration circuit into digital domain for less calibration power. With the advance of process technology, the analog circuit power does not benefit from the smaller technology length as shown in Fig. 2 [14]. To minimize the system power, the proposed signal-process-based calibration technique has compensation capability of 2dB gain error and 20 degree phase error. This balances the design efforts in analog circuit designs with the aid of only a little digital computation power. This also enlarges calibration tolerance to 10 times of existing design [4] with only 0.38mW power overhead by digital circuit.

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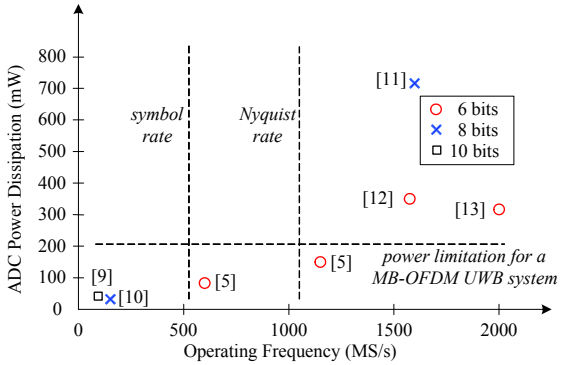


Fig. 1. ADC circuit power in different operating frequency and bit number.

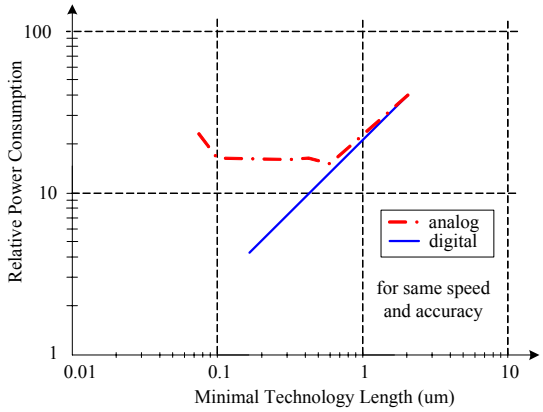


Fig. 2. Relative power consumption of analog and digital technology process in different technology length.

2. Proposed Design Architectures

Fig. 3 shows the proposed baseband transceiver. The transceiver achieves 53.3Mb/s ~ 480Mb/s data (de)modulation, including a mixed-radix 128-point FFT and divider-free channel equalizer for power saving [2][7][8]. This design also comprises synchronizer, IQM calibration, DSTC, and PTCG to solve the signal distortion caused by RF and channel effects. The all-digital PLL (ADPLL) generates 528MHz clock from 33MHz crystal, and PTCG generates 8-phase 528MHz clock for ADC and 1056MHz clock for DAC. It also generates 132MHz clock for baseband modules which achieve 528MS/s ~ 1056MS/s throughput with 4 ~ 8 parallel data paths. In the receiver path, the IQM calibration first bypasses received signals to the synchronizer. After packet detections, DSTC calculates preambles and gives Forward or Backward commands to PTCG. Each command results in ±236.7ps ADC clock phase shift to reach better signal sampling. After channel estimation in OFDM RX, IQM calibration extracts gain and phase errors from the estimated CFR and pilot values, and then compensates the IQM in the received signals.

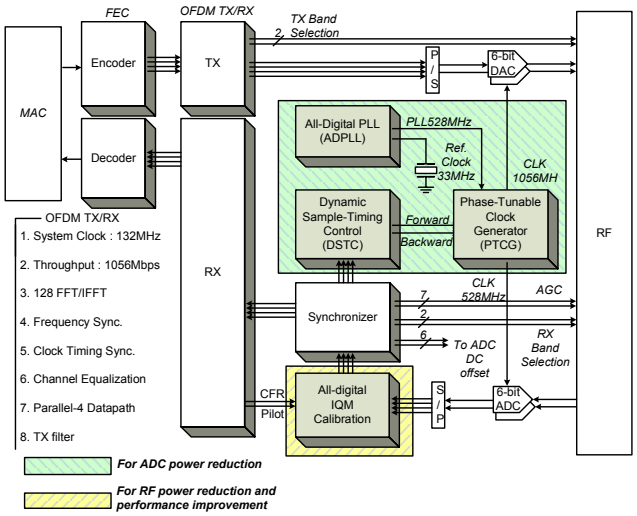


Fig. 3. System block diagram

Fig. 4 shows the architecture of proposed DSTC. ADC sampling timing will lead or lag 236.7ps respectively according to DSTC and PTCG, and every Forward or Backward command is sent during band transitions. This guarantees each OFDM symbol is sampled from the same clock phase. To limit less than 0.3dB SNR differences in PER performance due to different sampling timing, each clock period is divided into 8 sampling phases. After packet detection, DSTC takes 9 OFDM symbols in preamble to determine whether a signal is sampled at eye-open positions. For each OFDM symbol, signals are correlated and accumulated by their differences. This correlation results in complexity reduction due to only calculate real numbers. As long as overflow or underflow flag occurs, a forced-decision is made to PTCG. This effectively reduces half hardware cost and computation time, resulting in less power consumption.

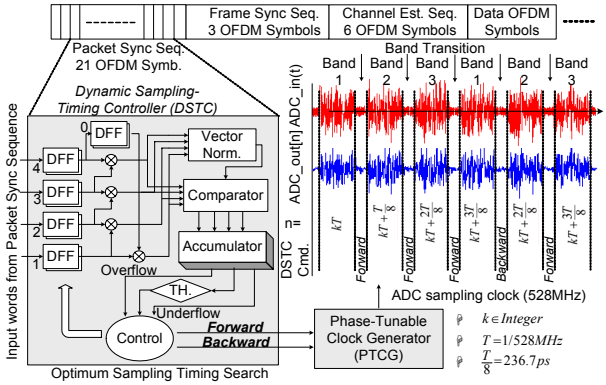


Fig. 4. The dynamic sampling-timing controller

Fig. 5 shows the architecture of IQM calibration circuit. With IQM effects, each OFDM subcarrier is interfered by the one from the symmetric index in spectrum, and the gain and phase values are thus distorted, resulting in non-square QPSK constellation. By this digital signal-process-based calibration, the transceiver automatically separates subcarrier interference and compensates signal distortion. To extract gain and phase errors, distorted pilots from two spectrum symmetric indices are subtracted from clean pilot values as shown in Fig. 2. Then the differences are compensated by estimated CFR, which is also IQM distorted. Therefore, a complex reciprocal is applied to eliminate this non-ideal channel estimation effect, and extracts the error parameters. For lower hardware cost, this reciprocal is also shared with IQM compensation circuit. The solvable IQM range with signals clipped by the 6-b I/Q ADC can be up to 2dB gain and 20 degree phase.

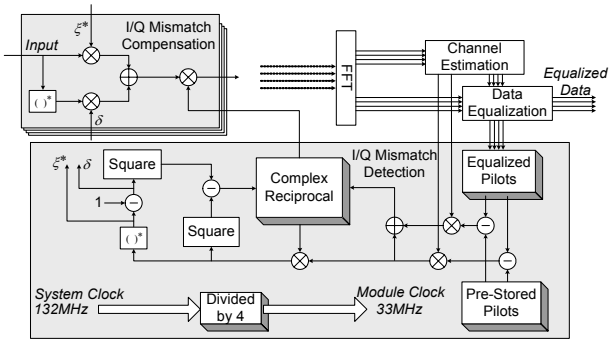


Fig. 5. Digital I/Q-mismatch calibration circuit

Fig. 6 shows the architecture of all-digital clock generation module. The ADPLL [3] generates 528MHz clock signal (PLL528) with 33MHz reference clock input. Then the ADMCG generates 528MHz eight-phase even-spaced clock signals (P[0] to P[7]) for the phase rotator. The phase rotator changes the output clock phase (CLK528) for the receiver ADC from P[n] to P[n+1] or P[n] to P[n-1] with baseband system's Forward or Backward commands respectively. Then the CLK528 is divided by four and serves as baseband system clock. To avoid possible glitches while phase selection change, the phase rotator converts the Forward command into seven times of Backward command. Hence the output phase will not have extra transitions during phase rotation. The generated multi-phase clock signals are also sent to the clock edge combiner to perform 2x frequency multiplication of PLL528 then generates the 1.056GHz clock signal (CLK1056) for the transmitter DAC.

In the proposed ADMCG architecture, the time-to-digital converter (TDC) is used to measure the period (T) of PLL528 and then selects a suitable delay range of the delay line. Thus the total delay line range can be limited into this range: 2.5T to 3.5T. This architecture avoid false-locked problem of DLL-based multi-phase clock generator and makes it possible to lock to harmonic of input clock period and can still get a correct multi-phase clock output in PVT variations. The proposed architecture actually helps to increase the minimum intrinsic delay limitations of the delay line, hence it increases the maximum operating frequency of the ADMCG. The proposed clock generation module is an all-digital and cell-based design, thus the proposed architecture can reduce both design time and circuit complexity and eases the difficulty when integration with baseband system.

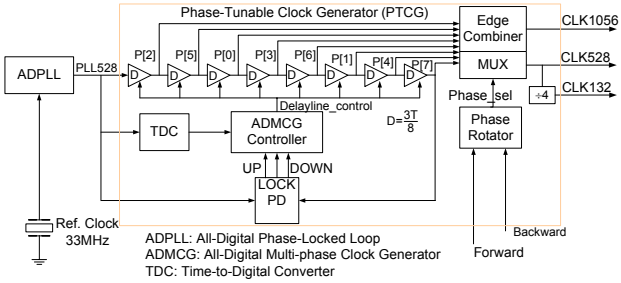


Fig. 6. The phase-tunable clock generator.

3. Simulation and Measurement Results

The proposed MB-OFDM UWB baseband transceiver is fabricated in 0.13μm 1P8M CMOS process. Fig. 7 and Fig. 8 show the simulated 480Mb/s PER performances and data constellation, including a gain error 2dB and phase error 20 degree in a AWGN channel. The equivalent transfer function or filter response of RF and ADC circuits are also included in this simulation platform and results. It is found that the necessary SNR to reach PER=8% is

about 13.2dB. When the digital IQM calibration is applied, a 3.2dB SNR improvement is acquired. Moreover, an additional 2.2dB SNR are improved with the DSTC for sample timing control. With IQM calibration, the gain and phase error are compensated, and the resulting signal constellation becomes a square QPSK distribution. With DSTC, the ADCs are able to sample signals with high signal integrity and little inter-symbol interference. Therefore, the resulting signal constellation after DSTC becomes much more centrally distributed. This not only consumes less ADC circuit power but also guarantees a better system performance.

Fig. 9 shows the measured signal constellation with I- and Q-path QPSK symbols. In the hardware implementation, data are represented in a limited wordlength. Therefore, the measured signal distribution is confined in a limited square region. Fig. 10 shows the measured receiver ADC sampling clock divided by 2. The output clock of ADPLL has rms jitter: 26ps and P_K-P_K jitter: 89ps.

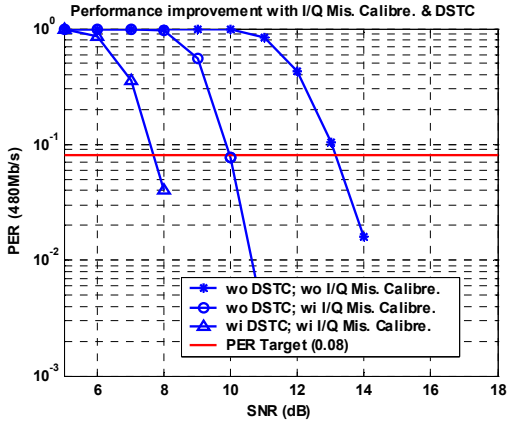
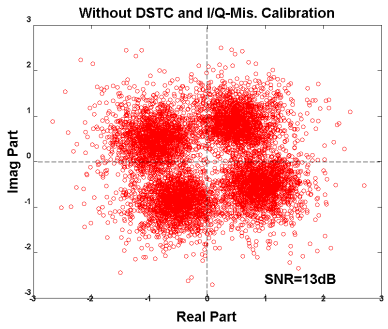
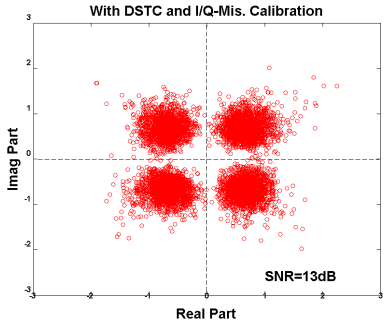


Fig. 7. Packet error rate (PER) performance @ 480 Mb/s data throughput



(a)



(b)

Fig. 8. Decoded signal constellation (a) before DSTC and IQM calibration (b) after DSTC and IQM calibration

After ADMCG and phase rotator, the jitter performance of ADC sampling clock is rms jitter: 23ps and P_K-P_K jitter: 60ps. Fig. 11 shows the power pie chart of the receiver circuit. The conventional necessary function blocks occupy about half the receiver power, including the synchronizer (timing and frequency synchronization), FFT, channel equalization, and signal dispreading. The other half includes the proposed IQM calibration, DSTC, and PTCG with ADPLL. It is found that the PTCG consumes a much higher power compared with the other functions. This is because a PTCG with ADPLL provides system clocks with 528MHz and 1056MHz, which are almost in operation, and deliver a higher power consumption ratio. However, every communication system requires a clock synchronizer providing the necessary system clocks. Therefore, we do not consider the PTCG as power overhead in the proposed design. To see the power reduction, Fig. 12 shows the necessary computing power without and with the proposed DSTC circuit. When the DSTC is not provided for sample timing control, the ADC has to operate at more than 2x symbol rate with higher operating power, say 320mW [5]. After the control circuit is included, we could reduce at least 140mW depending on the clocking rate reduction, which only pays a power overhead of 1.9mW. Fig. 13 shows the chip micro-photo, and Fig. 14 shows the Agilent 9300 tester for the proposed chip measurement. In Table I, we summarize the chip implementation and unique features in terms of dynamic sampling and IQM calibration.

4. Conclusion

Measured results show that the proposed design achieves maximum 480Mb/s data rate with 31.2mW power consumption. The power overhead is only 2.28mW with IQM calibration and DSTC, resulting in 5.4dB SNR improvement for typical 8% PER and 43.75% ADC power saving [5].

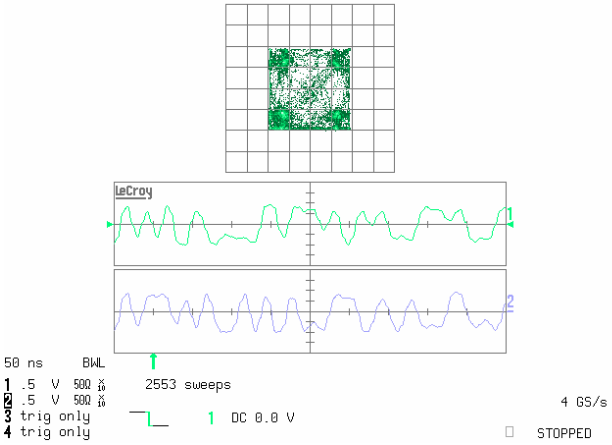


Fig. 9. Measured signal constellation after decoding

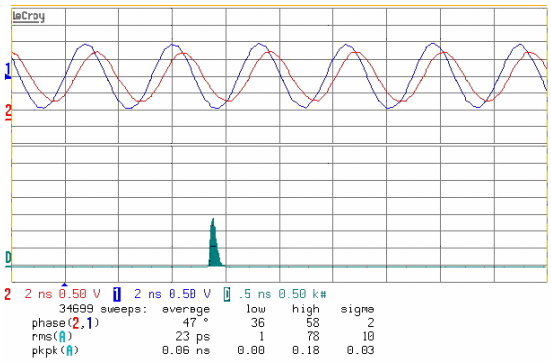


Fig. 10. PTCG measurement results

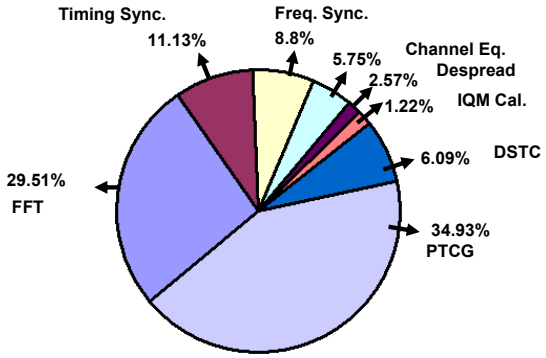


Fig. 11. Pie chart of RX signal power

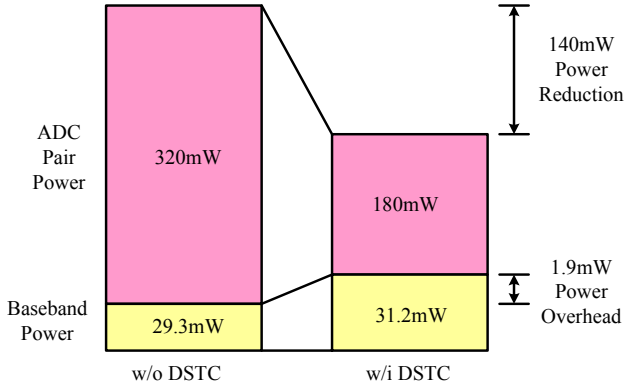


Fig. 12. Digital I/Q-mismatch calibration circuit

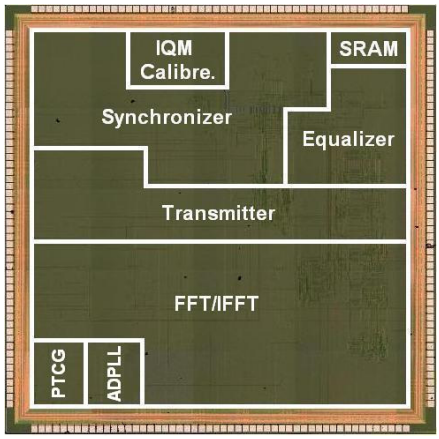


Fig. 13. The die photo of the implemented chip

Fig. 14. The Agilent 93000 tester for chip measurement

Table I

Technology	Std. 0.13um CMOS 1.2V core, 3.3V I/O
Die Size	3.975mm×3.980mm
Package	280-pin CQFP
Transistor Count	2.25M
Max. Data Rate	480Mb/s
Core Power @ 480Mb/s (TX/RX)	15.8/31.2mW
Gain Error Tolerance	2dB
Phase Error Tolerance	20 degree
PTCG Resolution	236.7ps

The implementation and function summary

References

[1] *Multi-band OFDM Physical Layer Proposal for IEEE 802.15 Task Group 3a*, IEEE Task Group 802.15.3a Merger-1, 2004.

[2] Jui-Yuan Yu, et. al, "A 31.2mW UWB Baseband Transceiver with All-Digital I/Q mismatch Calibration and Dynamic Sampling," *in Proc. 2006 IEEE Symposium VLSI Circuits*, pp. 290-291, Jun. 2006.

[3] Ching-Che Chung and Chen-Yi Lee, "An all-digital phase-locked loop for high-speed clock generation, " in *IEEE Journal of Solid-State Circuits*, Vol. 38, pp. 347-451, Feb. 2003.

[4] A. Ismail, A. Abidi, "A 3.1 to 8.2GHz Direct Conversion Receiver for MB-OFDM UWB Communications," *ISSCC Dig. Tech. Papers*, pp. 208-209, Feb. 2005.

[5] C. Sandner, et al., "A 6bit 1.2GSps Low-Power Flash-ADC in 013um Digital CMOS," in *IEEE Journal of Solid-State Circuits*, Vol. 40, pp. 1499-1505, Jul. 2005

[6] M. Bhardwaj, et al., "A 180MS/s, 162MS/s Wideband Three-Channel Baseband and MAC Processor for 802.11a/b/g," *ISSCC Dig. Tech. Papers*, pp. 454-455, Feb. 2005.

[7] Hsuan-Yu Liu, et al., "A 480Mb/s LDPC-COFDM-Based UWB Baseband Transceiver," *ISSCC Dig. Tech. Papers*, pp. 444-445, Feb. 2005.

[8] Yu-Wei Lin, et al., "A 1-GS/s FFT/IFFT processor for UWB applications," in *IEEE Journal of Solid-State Circuits*, Vol. 40, pp.1726-1735, Aug. 2005.

[9] Y. Masato, et al., "A 10b 125MS/s 40mW Pipelined ADC in 0.18µm CMOS," *ISSCC Dig. Tech. Papers*, pp.282-283, Feb. 2005.

[10] Hwi-Cheol Kim, et al., "A 30mW 8b 200MS/s Pipelined CMOS ADC Using a Switched-Opamp Technique," *ISSCC Dig. Tech. Papers*, pp. 284-285, Feb. 2005.

[11] T. Robert, et al., "A 1.8V 1.6GS/s 8b Self-Calibrating Folding ADC with 7.26 ENOB at Nyquist Frequency," *ISSCC Dig. Tech. Papers*, pp. 252-253, Feb. 2004.

[12] Peter Scholtens and Maarten Vertregt, "A 6-b 1.6-Gsample/s Flash ADC in 0.18-um CMOS Using Averaging Termination," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1599-1609, Dec. 2002.

[13] Xicheng Jiang, et al., "A 2GS/s 6b ADC in 0.18µm CMOS," *ISSCC Dig. Tech. Papers*, pp.322-323, Feb. 2003.

[14] Michiel Steyaert, "Analog Circuit Design towards Nanometer Technologies," *IEEE Asian Solid-State Circuits Conference*, Nov. 1-3, 2005.