An All-Digital On-Chip Silicon Oscillator with Automatic VT Range Selection Relative Modeling

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***Abstract*—In this paper, a 5MHz all-digital on-chip silicon oscillator is presented. The proposed on-chip oscillator uses a voltage and temperature classifier with the proposed linear calculator to compensate for voltage and temperature variations at chip run time. The maximum frequency errors with temperature and voltage variations are 0.21% and 0.97%, respectively. A systematic way to choose the standard cells for building the proposed design is also discussed in this paper.**

I. INTRODUCTION

In wireless sensor networks and biomedical devices, these systems operate with batteries and are highly integrated. Timing references are essential parts of these systems. In recent years, many researches had been devoted to develop CMOS-compatible on-chip oscillators [1]-[9] for replacing off-chip quartz crystal oscillators. The natural resonant frequency corresponding to the absolute value of RC or LC is commonly adopted for the oscillator design [3]. However, this oscillator requires canceling the temperature dependency of the passive components, and thus, the accuracy of the output frequency strongly depends on the process variations. A mobility-based frequency reference [1] and thermal-diffusivity-based frequency reference [2] have relatively small process variations, but their approaches have strong temperature dependency. Thus, they need accurate temperature sensors to compensate for the output frequency with temperature variations, and their approaches occupy a large chip area. In addition, the voltage variations are not considered in these approaches [1]-[3].

A frequency-locked-loop-based reference generator [4] uses a bias current circuit with a frequency-to-current converter to overcome temperature and voltage variations. However, the output frequency still depends on the variations of the resistance and the capacitance. Relaxation oscillators [5],[7] with power averaging feedback can tolerate both temperature and voltage variations. However, the resistive divider for the voltage reference require cancelling of temperature dependency, and a small voltage variations on the reference voltage (i.e. 2mV) can cause 0.4% frequency error [5], and thus, they are sensitive to the supply noise. Relaxation oscillator [6] requires a bias generator to overcome voltage and temperature variations. However, the bias generator occupies a large chip area.

An all-digital on-chip oscillator with the relative reference modeling is proposed in [9]. The digital approach makes it easy to design the on-chip oscillator. However, a high order polynomial is required to minimize the modeling error, and thus, a mapper is required to reduce the area cost. In this paper, the proposed design also uses the relative modeling to build up the on-chip oscillator. However, a voltage and temperature classifier is proposed to reduce the modeling error of [9] to achieve a better accuracy of the output frequency. The proposed design can operate with a low supply voltage and very suitable for low-power and low-cost system-on-a-chip (SoC) application.

II. RELATIVE REFERENCE MODELING

The propagation delay time of the logic cells are easily affected by process, voltage, and temperature (PVT) variations. If we choose any three logic cells from the standard cell library, and one of them uses as a reference delay cell (RDC), and the other cells use as the compare delay cell 1 (CDC1) and the compared delay cell 2 (CD2). The delay ratio between these logic cells can be expressed as

$$R1(P,V,T) = \frac{D_{RDC}(P,V,T)}{D_{CDC1}(P,V,T)} \quad (1)$$

$$R2(P,V,T) = \frac{D_{RDC}(P,V,T)}{D_{CDC2}(P,V,T)} \quad (2)$$

where $D_{RDC}(P,V,T)$, $D_{CDC1}(P,V,T)$, and $D_{CDC2}(P,V,T)$ are the delay time of the RDC, CDC1, and CDC2, respectively.

For a fixed supply voltage (V) and certain process corner (P), $D_{RDC}(P,V,T)$ and $D_{CDC1}(P,V,T)$ are both increased and decreased with temperature variations. Thus, the range of R1(P,V,T) means the temperature coefficients difference between RDC and CDC1. Therefore, if there exists a RDC and CDC1 pair, which the range of the R1(P,V,T) at all process corners with different voltages are not overlapped. Then, R1(P,V,T) can be used to roughly determine the supply voltage of the chip. Similarly, for a fixed temperature (T) and

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certain process corner (P), $D_{RDC}(P,V,T)$ and $D_{CDC2}(P,V,T)$ are both increased and decreased with voltage variations. Thus, if there exists a RDC and CDC2 pair, which the range of the R2(P,V,T) at all process corners with different temperatures are not overlapped. Then, R2(P,V,T) can be used to roughly determine the temperature of the chip. In this paper, the R1(P,V,T) and R2(P,V,T) are used by the proposed voltage and temperature classifier, and the accuracy of the output frequency of the on-chip ring oscillator can be significantly improved.

III. System Architecture

A. Delay Ratio Estimator

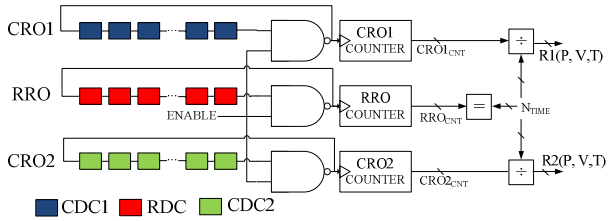

Figure 1. The proposed delay ratio estimator.

The block diagram of the proposed delay ratio estimator (DRE) is shown in Fig. 1. In DRE, three logic cells, RDC, CDC1, CDC2 are used to create three ring oscillators, the reference ring oscillator (RRO), the compared ring oscillator 1 (CRO1), and the compared ring oscillator 2 (CRO2), respectively. The output of the ring oscillator is connected to the counter to record the oscillation cycles of the oscillator. The value of these counters can be used to calculate the delay ratio R1(P,V,T) and R2(P,V,T) as follows:

$$R1(P,V,T)=\frac{CRO1_{CNT}}{RRO_{CNT}} \tag{3}$$

$$R2(P,V,T)=\frac{CRO2_{CNT}}{RRO_{CNT}} \tag{4}$$

where $CRO1_{CNT}$, $CRO2_{CNT}$ and RRO_{CNT} are the output of the CRO1 counter, the CRO2 counter, and the RRO counter, respectively. The RRO counter will count from 0 to N_{TIME}, and then the three ring oscillators are stopped. The value of N_{TIME} is set to 2047, thus the delay ratio R1(P,V,T) and R2(P,V,T) can be computed without divider circuits.

B. Digitally Controlled Oscillator

The proposed DCO architecture is shown in Fig. 2. The output of the RRO triggers the DCO counter, and when the output value of the DCO counter equals to the input control code (DCO_CODE), a pulse is generated, and then the DCO counter is reset. To generate the output clock with a 50% duty cycle, a divided-by-2 circuit is added before output. The output frequency of the DCO can be expressed as follows:

$$F_{DCO}=\frac{1}{P_{RRO(P,V,T)}\times DCO\_CODE\times 2} \tag{5}$$

where $P_{RRO}(P,V,T)$ is the period of the RRO, and F_{DCO} is the output frequency of the DCO. The period of RRO is easily affected by PVT variations, thus the input control code (DCO_CODE) can be used to adjust the output frequency with PVT variations.

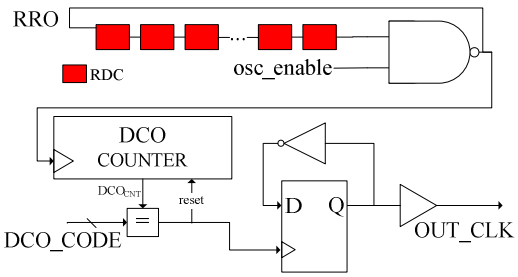

Figure 2. The proposed DCO architecture.

C. Cell Selection Rules for Delay Ratio Estimator

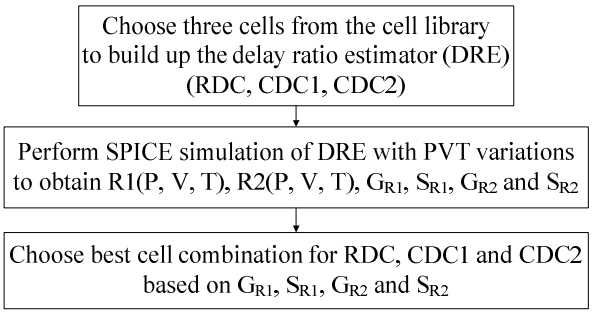

Figure 3. Flow chart of how to choose cells from the cell library.

Fig. 3 shows the cell selection flow chart for RDC, CDC1, and CDC2. At first, any three logic cells are selected from the standard cell library to build up the delay ratio estimator. Subsequently, we need to perform SPICE simulation of the DRE with PVT variations to obtain delay ratios, R1(P,V,T) and R2(P,V,T). In this paper, the voltage varies from V_1 to V_5 (V_1=0.90V, V_2=0.95V, V_3=1.00V, V_4=1.05V, and V_5=1.10V), and temperature varies from T_1 to T_4, (T_1=0°C, T_2=25°C, T_3=50°C, and T_4=75°C). In addition, the process variation includes typical process corner (TT), best process corner (FF), and worst process corner (SS). Therefore, it needs to simulate the DRE in totally 60=(3×5×4) different P,V,T combinations.

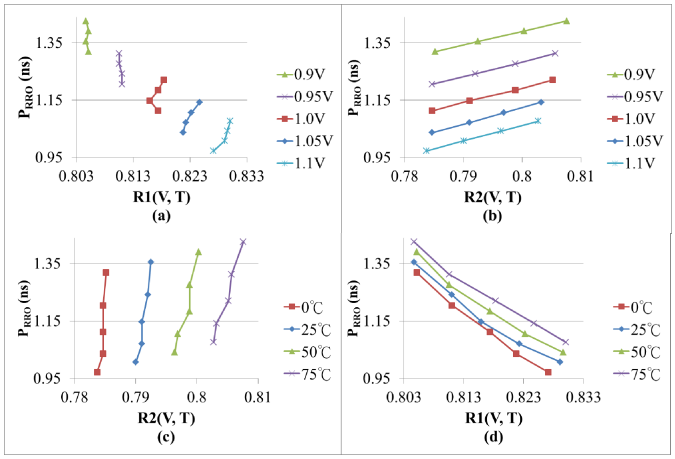

Figure 4. Delay ratios R1(V, T) and R2(V,T) versus P_{RRO} (V,T) in typical process corner.

Fig. 4 shows the delay ratios R1(V,T) and R2 (V,T) versus the period of the RRO, $P_{RRO}(V,T)$ in typical process corner. In Fig. 4(a), with a fixed voltage value, the delay ratio R1 varies

with temperature variations. ΔTT_{R1n} of Eq. 6 means the spacing between the R1 delay ratio curves with voltage V_n and voltage V_{n+1} in typical process corner. In Fig. 4(c), with a fixed temperature value, the delay ratio R2 varies with voltage variations. ΔTT_{R2j} of Eq. 7 means the spacing between the R2 delay ratio curves with temperature T_j and temperature T_{j+1} in typical process corner. The values of ΔTT_{R1n} and ΔTT_{R2j} should be greater than zero, so that the delay ratios R1(V,T) and R2(V,T) can be used to roughly estimate the supply voltage and operation temperature at chip run time. Therefore, if the DRE fails to meet this requirement, the current cell combinations are dropped, and then, we need to choose other cell combinations and repeat the SPICE simulation of the DRE again.

$$\Delta TT_{R1n} = MIN(R1(TT, V_{n+1}, T)) - MAX(R1(TT, V_n, T)) \quad (6)$$

$$\Delta TT_{R2j} = MIN(R2(TT, V, T_{j+1})) - MAX(R2(TT, V, T_j)) \quad (7)$$

$$\Delta TT_{R1} = \sum_{n=1}^{4} \Delta TT_{R1n} \quad (8)$$

$$\Delta TT_{R2} = \sum_{j=1}^{3} \Delta TT_{R2j} \quad (9)$$

$$G_{R1} = (\Delta TT_{R1} + \Delta SS_{R1} + \Delta FF_{R1}) \quad (10)$$

$$G_{R2} = (\Delta TT_{R2} + \Delta SS_{R2} + \Delta FF_{R2}) \quad (11)$$

$$S_{R1} = Std(\Delta TT_{R1}, \Delta SS_{R1}, \Delta FF_{R1}) \quad (12)$$

$$S_{R2} = Std(\Delta TT_{R2}, \Delta SS_{R2}, \Delta FF_{R2}) \quad (13)$$

The DRE should be simulated with different process corners. In Eq. 10, G_{R1} of the current DRE is defined as the summation of ΔTT_{R1}, ΔSS_{R1}, and ΔFF_{R1}, where ΔTT_{R1}, ΔSS_{R1}, and ΔFF_{R1} are the summation of the R1 curve spacing in typical process corner, worst process corner, and best process corner, respectively. Similarly, G_{R2} of the current DRE is defined as the summation of ΔTT_{R2}, ΔSS_{R2}, and ΔFF_{R2}, where ΔTT_{R2}, ΔSS_{R2}, and ΔFF_{R2} are the summation of the R2 curve spacing in typical process corner, worst process corner, and best process corner, respectively. In Eq. 12, S_{R1} is the standard deviation of ΔTT_{R1}, ΔSS_{R1}, and ΔFF_{R1}, and S_{R2} is the standard deviation of ΔTT_{R2}, ΔSS_{R2}, and ΔFF_{R2}. We need to compute G_{R1}, G_{R2}, S_{R1}, and S_{R2} of all possible cell combinations, and the cell combination with largest values of G_{R1} and G_{R2}, and smallest values of S_{R1}, S_{R2} is the best choice for design the DRE. However, if we cannot find this best choice, the cell combination with a larger G_{R1}value and smaller S_{R1} value is a better choice. In this paper, we use a 90nm cell library to implement the DRE, and the best cell combination is (AND3X1, NAND4XL, DLY1X1) for (RDC, CDC1, CDC2).

D. On-Chip Oscillator with Relative Modeling

The proposed on-chip ring oscillator architecture which uses the relative reference modeling is shown in Fig. 5. It is composed of a delay ratio estimator, a voltage classifier, a temperature classifier, a linear calculator, and a digitally controlled oscillator (DCO). The DRE estimates the R1(V,T) and the R2(V,T) at chip run time under voltage and temperature variations. In this paper, we need to measure the values of R1(V,T), R2(V,T), and P_{RRO}(V,T) with five different voltages (V_1 to V_5) and four different temperatures (T_1 to T_4), Therefore, it needs to measure the values of R1(V,T), R2(V,T), and P_{RRO}(V,T) in totally 20 different (V,T) cases.

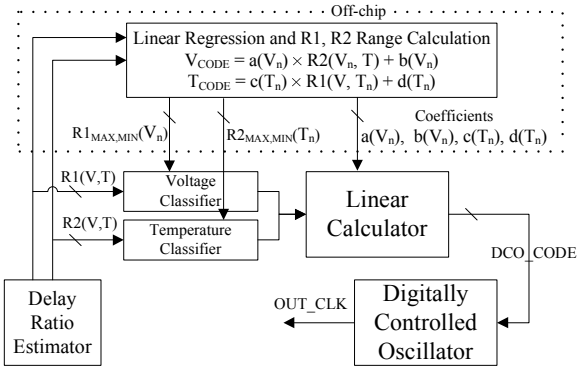

Figure 5. The proposed on-chip oscillator architecture.

The maximum value and minimum value of R1(V_n, T) at voltage V_n with temperature variations (T_1 to T_4) will be found in the off-chip process, and are stored as $R1_{MAX}(V_n)$ and $R1_{MIN}(V_n)$, where V_n is V_1 to V_5. Similarly, the maximum value and minimum value of R2(V, T_n) at temperature T_n with voltage variations (V_1 to V_5) will be found in the off-chip process, and are stored as $R2_{MAX}(T_n)$ and $R2_{MIN}(T_n)$, where T_n is T_1 to T_4. In the off-chip process, we perform the linear regression on the R2(V_n, T) versus DCO_CODE at voltage V_n to obtain the coefficients $a(V_n)$ and $b(V_n)$, where V_n is V_1 to V_5. In addition, we also perform the linear regression on the R1(V, T_n) versus DCO_CODE at temperature T_n to obtain the coefficients $c(T_n)$ and $d(T_n)$, where T_n is T_1 to T_4. Thus there are totally 18 coefficients stored in the linear calculator for further voltage and temperature compensation at chip run time.

When the values of $R1_{MAX}(V_n)$, $R1_{MIN}(V_n)$, $R2_{MAX}(T_n)$, and $R2_{MIN}(T_n)$, $a(V_n)$, $b(V_n)$, $c(T_n)$, and $d(T_n)$ for V_1 to V_5 and T_1 to T_4 are determined in the off-chip process, the proposed on-chip oscillator are now ready for generating the required target frequency (F_{DCO}). At chip run time, the DRE estimates R1(V,T) and R2(V,T) with a unknown supply voltage (V) and a unknown operation temperature (T). The voltage classifier uses the $R1_{MAX}(V_n)$ and $R1_{MIN}(V_n)$ to roughly estimate the unknown supply voltage. For example, if R1(V,T) is smaller than $R1_{MAX}(V_2)$ but is larger than $R1_{MIN}(V_2)$, and then, the current supply voltage can be estimated as V_2. The temperature classifier uses the $R2_{MAX}(T_n)$ and $R2_{MIN}(T_n)$ to roughly estimate the unknown operation temperature. For example, if R2(V,T) is smaller than $R2_{MAX}(T_3)$ but is larger than $R2_{MIN}(T_3)$, and then, the current operation temperature can be estimated as T_3. Then, the linear calculator uses Eq. 14 and Eq. 15 to calculate two DCO control codes (V_{CODE} and T_{CODE}). Finally, the DCO control code for the DCO is the average of the V_{CODE} and T_{CODE}. (i.e. DCO_CODE = (V_{CODE} + T_{CODE})/2).

$$V_{CODE} = a(V_n) \times R2(V_n, T) + b(V_n) \quad (14)$$

$$T_{CODE} = c(T_n) \times R1(V, T_n) + d(T_n) \quad (15)$$

In some special cases, for example, if R1(V,T) is smaller than $R1_{MIN}(V_3)$ but is larger than $R1_{MAX}(V_2)$, the voltage classifier can only determine the unknown supply voltage is between V_2 and V_3. In this case, the V_{CODE} can be computed

by $[a(V_2)+a(V_3)]/2 \times R2\ (V, T) + [b(V_2)+b(V_3)]/2$. Similarly, if the temperature classifier determines the unknown operation temperature is between T_2 and T_3, the T_{CODE} can be computed by $[c(T_2)+c(T_3)]/2 \times R1\ (V, T) + [d(T_2)+d(T_3)]/2$.

IV. Experimental Results

The proposed on-chip oscillator circuit is implemented in a standard 90nm 1P9M CMOS process. The operating voltage ranges from 0.90V to 1.10V, and temperature range is from 0°C to 75°C. The layout of the test chip is shown in Fig. 6. The active area is 180µm ×180µm, and chip area including I/O pads is 830µm ×830µm.

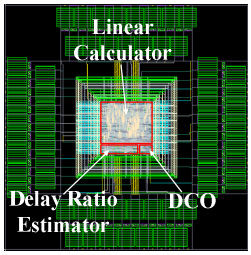

Figure 6. Layout of the test chip.

Fig. 7 shows the output frequency of the proposed on-chip oscillator with PVT variations. The target frequency is 5MHz. Table I shows the comparisons with the state-of-the-art designs. The frequency error of the proposed on-chip oscillator with temperature variations is 0.21% in typical process corner, which is smaller than prior researches. Although [2] has a smaller temperature variations, it does not tolerate the voltage variations. The maximum frequency error of the proposed design with voltage variations is 0.97% in typical process corner. Relaxation oscillators [5],[7] can achieve relatively small voltage variations. However, a small voltage variations on the reference voltage (i.e. 2mV) can cause 0.4% frequency error [5], and thus, they are sensitive to the supply noise. The maximum output frequency error with PVT variations ranges from -2.83% to +2.49%.

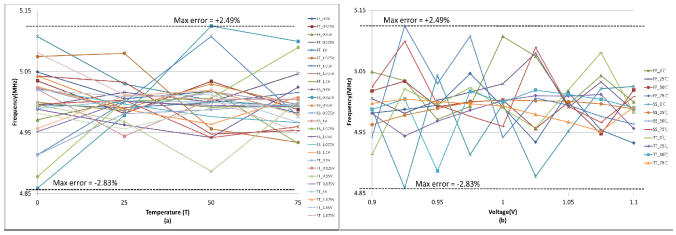

Figure 7. Output frequency with PVT variations (a) x-axis is tempereature (b) x-axis is voltage.

V. Conclusion

The proposed on-chip oscillator with a relative modeling uses the voltage and temperature classifier to roughly estimate the supply voltage and operation temperature at chip run time. Therefore, the frequency error can be significant reduced by a linear equation-based compensation approach. The proposed design can be implemented by standard cells, and we also propose the cell selection rules to choose the cells for the delay ratio estimator. As a result, the proposed design provides a systematic way to automatically generate the on-chip oscillator with PVT variations tolerance. Thus the proposed design can operate with a low supply voltage, and is very suitable for low-power and low-cost system-on-a-chip application.

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TABLE I

	This work	[1]JSSC'11	[2]JSSC'12	[3]JSSC'09	[4]ESSCIRC'09	[5]JSSC'10	[7]VLSIC'10	[8]VLSIC'09	[9]TVLSI'12
Technology(nm)	90	65	160	65	350	180	65	180	90
Frequency(MHz)	5	0.15	16	6	30	14	6	10	5
Temp. Range	0 ~ 75	-55 ~125	-55 ~ 125	0 ~ 120	-20 ~ 100	-40 ~ 125	-40 ~ 125	-20 ~ 100	0 ~ 75
Vari. with Temp.	0.21%	0.5%	0.1%	0.6%	0.7%	0.75%	0.20%	0.4%	1%
VDD Range	0.9~1.1	fixed 1.2v	fixed 1.8v	fixed 1.2v	fixed 1.8v	1.7 ~ 1.9	1.15 ~ 1.35	1.2 ~ 3.0	0.9 ~1.1
Vari. with VDD	0.97%	N/A	N/A	N/A	N/A	0.16%	0.26%	0.05%	1%
power(mW)	1.42	0.051	2.1	0.066	0.18	0.045	0.1	0.08	0.65
area(mm^2)	0.0324	N/A	0.5	0.03	0.08	0.04	0.021	0.09	0.04
Design Approach	cell-based	full-custom	full-custom	full-custom	full-custom	full-custom	full-custom	full-custom	cell-based