An All-Digital Smart Temperature Sensor with Auto-Calibration in 65nm CMOS Technology

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***Abstract*— A novel fully digital CMOS smart temperature sensor with auto-calibration circuit in 65nm CMOS technology is presented. The proposed auto-calibration circuit can greatly reduce the temperature calibration efforts, and therefore it is very suitable for on-chip dynamic thermal management applications. The power consumption of the proposed circuit is 55μW with 1.0V supply.**

I. INTRODUCTION

In recent years, the advanced CMOS process makes it possible to integrate many designs into a single chip. When multiple chips are integrated and fabricated on the same wafer, the power consumption wasted on the I/O buffers and the board-level interconnection parasitic RCs can be saved. However, system integration also increases design complexity and power density. As a result, on-chip thermal sensing or monitoring is very important for system reliability and dynamic thermal management [1-4].

Thermal monitoring using on-chip thermal sensors provides the run-time thermal profile of a system, and when hot spot occurs, the thermal management circuit can send request to the system controller to stop the current operation or to slow down the system clock frequency so that the chip temperature can be kept below the specified temperature limitation, and therefore the reliability of the system can be improved.

Many temperature sensors are uniformly placed on the chip to detect the local temperature variations of the chip in run-time. The requirements for these temperature sensors are small area, low-power consumption, and easy calibration. Temperature sensors should have extreme low-power consumption to avoid self-heating effects to the system. And temperature sensors must be easy to perform absolute temperature calibration and have sufficient conversion rate (> 1000 samples/sec) to monitor the run-time thermal profile of a system.

Traditionally, the BJT-based smart temperature sensors [7] are widely used in many applications. The BJT-based smart temperature sensor converts the measuring temperature into a voltage or current first, and then the analog-to-digital converter (ADC) transforms voltage or current information into digital codes. However, the BJT-based smart temperature sensor usually has large chip area and high power consumption due to the ADC circuit and the band gap reference voltage circuit. And the BJT-based smart temperature sensor also needs the second order curvature correction circuit and post-silicon transistor trimming to improve the accuracy of temperature measurement. Since there are many temperature sensors on the chip, it is not possible to perform absolute temperature calibration and post-silicon transistor trimming for every temperature sensors. And it also takes more efforts to integrate the analog circuits with the digital circuits. As a result, the BJT-based smart temperature sensors are not suitable for dynamic thermal management in system-on-a-chip (SoC).

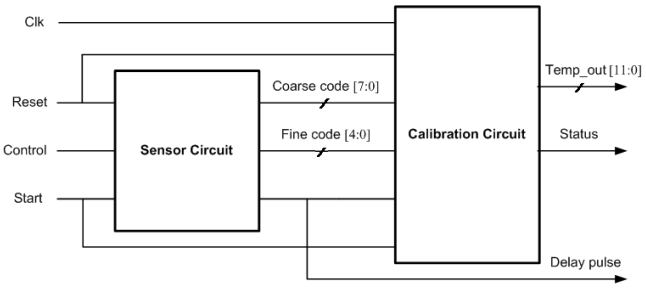

Figure 1. The block diagram of the proposed smart temperature sensor.

The all-digital time-domain smart temperature sensor which uses the time-to-digital converter (TDC) to quantize the delay pulse into temperature information is proposed in [5-6]. The full-digital architecture make it is easy to be ported to different processes in a short time, and it is also easy to be integrated into the digital systems. However, the power consumption of the all-digital temperature sensor [5] with 1,000 samples/sec conversion rate is at milli-watt level which is too much for thermal management applications. And the temperature sensors [5-6] still need to perform two temperature points calibration before the temperature sensors can be used. Since there are many temperature sensors on the chip, and therefore how to reduce the calibration cost of the temperature sensor array becomes very important now.

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Thus the temperature sensor with dual DLLs to perform one temperature point calibration is proposed in [8]. The reference clock with a multi-phase delay line can generate a fixed delay in PVT variations to calibrate the temperature errors. However, the temperature sensor with dual DLLs occupied too much chip area with high power consumption at milli-watt level.

In this paper, an all-digital smart temperature sensor with auto-calibration functionality with 65nm technology is presented. The proposed temperature sensor can perform auto-calibration in room temperature when system is reset. After the auto-calibration, the run-time thermal profile of a system can be monitored at 10,000 samples/sec conversion rate with micro-watt level power consumption. Since the proposed temperature sensor eliminates the two temperature points calibration on every temperature sensors, it is very suitable for current thermal management applications in SoC era.

The rest of the paper is organized as follows. Section II describes the overall operation of the proposed temperature sensor with auto-calibration circuit. The proposed temperature sensor circuit is discussed in Section III. Section IV explains the proposed auto-calibration circuit used in this design. Section V shows the experimental simulation results of the proto-type chip. Finally, Section VI concludes with a summary.

II. Overall Circuit Description

The block diagram of the proposed smart temperature sensor with auto-calibration circuit is shown in Fig. 1. The operation of the proposed smart temperature sensor is partitioned into two phases: the auto-calibration phase and the real temperature measurement phase. After system is reset, the temperature sensor enters auto-calibration phase, and in this phase, the on-chip temperature is assumed to the room temperature at 25°C.

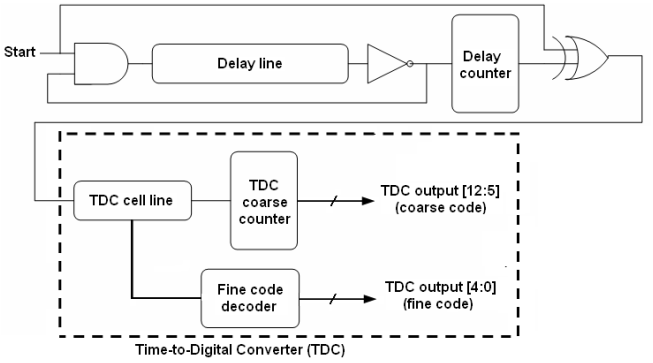

Figure 2. The proposed smart temperature sensor circuit.

Then when the signal "Start" is enabled in this phase, the sensor circuit will produce a digital code which is proportional to the absolute temperature (PTAT) at room temperature 25°C. Then this code is sent to the calibration circuit and saved as the reference code. After the reference code is sent to the calibration circuit, the temperature sensor is ready for run-time real temperature measurement. Then every time when the signal "Start" is enabled, the sensor circuit measures current temperature information and it outputs digital codes (coarse_code[7:0], fine_code[4:0]) to the calibration circuit to calculate the temperature near the on-chip temperature sensor.

III. Sensor Circuit Implementation

The architecture of the proposed sensor circuit is shown in Fig. 2. It is composed of the cyclic delay line, the TDC cell line, the TDC coarse counter and the TDC fine code decoder.

The following subsections describe the components of the proposed temperature sensor circuit in detail.

A. Cyclic Delay Line

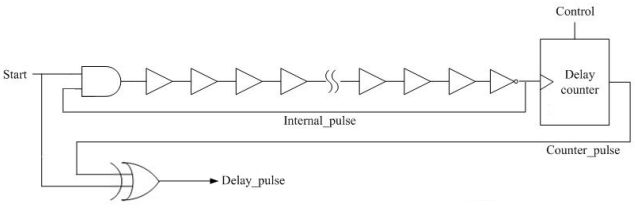

Figure 3. The proposed cyclic delay line.

Fig. 3 shows the architecture of the proposed cyclic delay line, and in Fig. 4, the timing diagram of the cyclic delay line is shown. The cyclic delay line is a temperature-to-pulse generator. It is used to generate a pulse and its width is proportional to the absolute temperature (PTAT) [5]. The cyclic delay line will start to oscillate after the signal "Start" is enabled. The delay counter counts the number of positive edges of the signal "internal_pulse". When the delay counter reaches the specified number, the signal "counter_pulse" will be enabled. Then the signal "Start" and the signal "counter_pulse" are inputted to the XOR gate to generate the signal "delay_pulse" for the TDC.

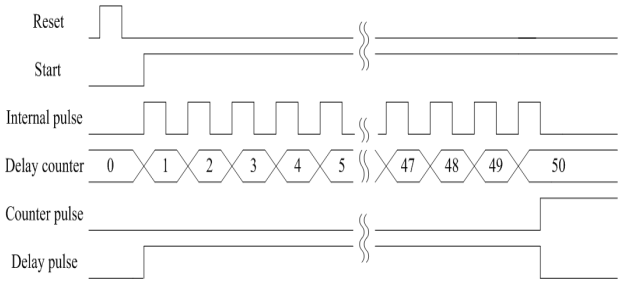

Figure 4. The timing diagram of the cyclic delay line.

The pulse width of the signal "delay_pulse" can be controlled by the delay counter, and the pulse width should be wide enough for the next stage TDC to quantize it into digital codes. In addition to the above viewpoint, more delay cells used in the cyclic delay line means that the "internal_pulse" output frequency is reduced, and the power consumption of the cyclic delay line is reduced, too. But if the number of delay cells is increased, the area of the cyclic delay is also increased.

B. Time-to-Digital Converter

After the PTAT pulse is generated by the cyclic delay line. The time-to-digital converter is used to quantize the pulse

width information into digital codes. The proposed TDC is composed of the coarse counter and the fine code decoder to achieve high resolution quantization.

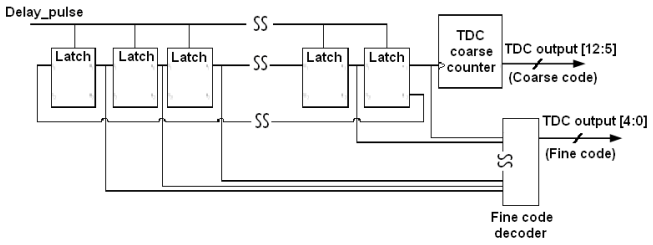

Figure 5. The circuit of the time-to-digital converter (TDC).

The TDC cell line is shown in Fig. 5. In the proposed TDC, 16 latches are used to compose the TDC cell line. When the signal "delay_pulse" is enabled, then all latches in the TDC cell line are turned on and the TDC cell line starts to oscillate. The TDC coarse counter counts the arrival positive edges to generate the TDC coarse code. This operation is continued until the signal "delay_pulse" is disabled. Then the residual pulse width information can be generated after the fine code decoder. Then the output of the TDC coarse counter and the fine code decoder are combined as the TDC_output[12:0].

IV. Calibration Circuit Implementation

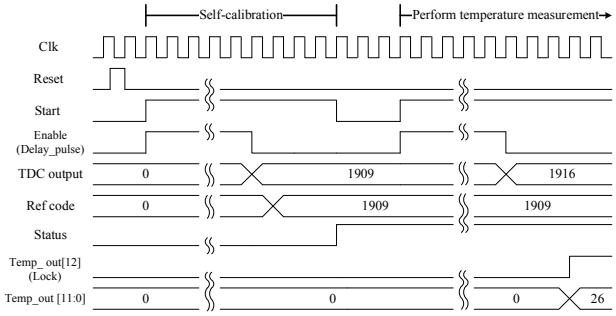

Figure 6. Timing diagram of the calibration circuit.

The operation of the calibration circuit is shown in Fig. 6. The proposed temperature sensor circuit is composed of the cyclic delay line and the TDC. Although the temperature information is already converted into the digital codes, these digital codes must be calibrated before output. This because the process, voltage, and temperature variations make it impossible to create a fixed mapping between the absolute temperature values (°C) and the TDC's output codes.

Hence when system is reset, the on-chip temperature is assumed to room temperature at 25°C. Thus the reference code for room temperature can be generated. In Fig. 6, when the signal "Start" is enabled in auto-calibration phase, the first output of the sensor circuit is stored as reference code for the calibration circuit. After the self-calibration has completed, the signal "Status" is pulled up to indicate that the sensor is ready for temperature measurement. Then when the temperature of the sensor circuit is changed, the new temperature value can be calculated from the difference between reference code and current TDC output code.

In the proposed temperature sensor, the TDC's output codes are assumed to be linear with the temperature. Hence the SPICE circuit simulation is performed to determine the slope of the line in typical case. We can use this line as the temperature output predictor. Hence when the TDC's output code at room temperature (25°C) is generated. The offset of this line in run-time is determined, and the slope of this line is assumed unchanged. As a result, the difference between the reference code and the current TDC output code can be used to calculate the current temperature in centigrade degree.

After the calculation is finished, the lock signal will be pulled up to indicate that the temperature output is valid. In practical applications, one of the on-chip temperature sensors can use the traditional two temperature point calibration. And the temperature at system reset can be determined from this calibrated sensor. As a result, the reference code generation is more accurate in other non-calibrated temperature sensors.

V. Experimental Result

The proto-type temperature sensor is fabricated on a standard performance (SP) 65nm CMOS process. In this chip, the cyclic delay line is composed of 50 delay cells, and the delay counter number is 50.

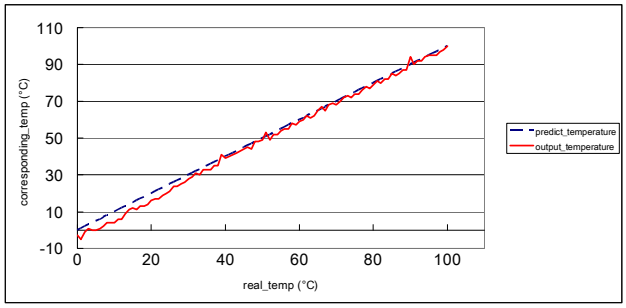

Figure 7. The sensor's output temperature with real temperature.

Fig. 7 shows the simulation results of the proposed sensor circuit in different temperatures ranges from 0°C to 100°C. The line "predict_temperature" means the ideal temperature predictor, and the line "output_temperature" means the real output temperature value of the proposed sensor circuits. The difference between these two lines is often caused by non-linearity of the proposed temperature sensor, the bit resolution in calibration circuit, and the TDC resolution limitation.

However, the measured temperature errors are further increased by the process and voltage variations. In Fig. 8, the temperature errors in best case, typical case, and worst-case conditions are shown. The maximum temperature error of the proposed temperature sensor is always below ±10.0°C which is sufficient in dynamic thermal management applications. And the layout of the test chip is shown in Fig. 9.

Table I. lists the comparisons of recent smart temperature sensors. In all-digital smart temperature sensors [5-6], the proposed design can achieve higher conversion rate with lower power consumption. And the two-point temperature calibration is eliminated in the proposed design with auto-calibration. Although the temperature error is very small (±

TABLE I. COMPARISONS OF RECENT SMART TEMPERATURE SENSORS.

Sensor	Resolution (°C)	Error (°C)	Calibration	Power	Area (mm^2)	Conversion Rate (samples/s)	Temperature Range (°C)	CMOS Technology
[5]	0.16	-0.7 ~ +0.9	Two-point	0.49mW@ 3.3V	0.175	1,000	0 ~ 100	0.35 µm
[6]	0.058	-1.5 ~ +0.8	Two-point	8.4 µW@ 2.5V	N/A	2	0 ~ 75	FPGA
[7]	0.01	±0.1 (3σ)	One-point with Post-silicon Trimming	247 µW@ 3.3V	4.5	10	-55 ~ 125	0.7 µm
[8]	0.66	-1.8 ~ +2.3	One-point with Dual DLLs	12 mW@ 1.2V	0.16	5,000	0 ~ 100	0.13 µm
proposed	0.143	±10.0	Auto Calibration	55 µW@ 1.0V	0.01	10,000	0 ~ 100	65 nm

0.1°C) in [7], this BJT-based temperature sensor is not suitable for dynamic thermal management applications. And in [8], the high power consumption and large chip area makes it is also not suitable for dynamic thermal monitoring.

VI. CONCLUSION

A novel fully digital CMOS smart temperature sensor with auto-calibration circuit has been developed with 65nm CMOS technology. It has tiny chip area and low power consumption, and the traditional two temperature points calibration can be eliminated makes it very suitable for on-chip dynamic thermal management applications in SoC. The maximum temperature error is below ±10.0°C in worst-case conditions.

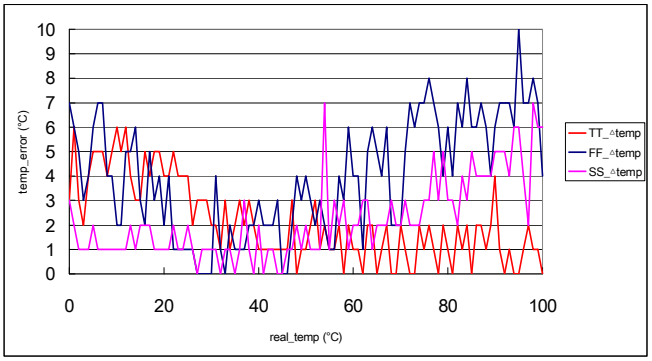

Figure 8. Temperature measurement errors of the proposed sensor.

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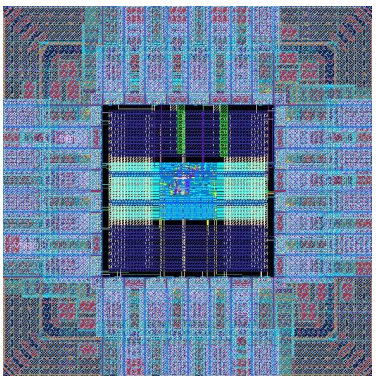

Figure 9. Layout of the proposed smart temperature sensor