AN ALL-DIGITAL PHASE-LOCKED LOOP FOR HIGH-SPEED CLOCK GENERATION

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ABSTRACT

An all-digital phase-locked loop (ADPLL) for high-speed clock generation is presented in this paper. The proposed ADPLL architecture can be implemented with standard cells. And the ADPLL implemented in a 0.35μm 1P4M CMOS process can operate from 40MHz to 540MHz. The p-p jitter of the output clock is less than ±170ps, and the rms jitter of the output clock is less than 39ps. A systematic way to design the ADPLL with specified standard cell library is also introduced. The proposed ADPLL can easily be ported to different processes in a short time. Thus it can reduce the design time and design complexity of ADPLL, making it very suitable for System-On-Chip (SoC) applications.

1. INTRODUCTION

Phase-Locked Loops (PLL's) has been commonly used in data communication and microprocessor. It can be applied to Clock and Data Recovery (CDR) circuits and frequency synthesis applications. In conventional designs, PLL's is often designed by analog approaches. But since analog PLL's have to overcome the noise coupling, signal shading, and power supply noise effects, it's difficult to be integrated into system. All-Digital Phase-Locked Loops (ADPLL's) [1-4] have been proposed to overcome those disadvantages of analog PLL's and reduce the turn around time for system integration.

There are two major problems needed to be considered carefully when designing the ADPLL. One is how to design a wide operating range and high resolution Digital-Controlled Oscillator (DCO), the other problem is how to speedup the frequency acquisition and phase acquisition, and reduce the clock jitter comes from reference clock. In [1], a binary-weighted MOS width DCO is proposed to achieve high frequency resolution. But since the area of DCO in [1] takes a large area, a 4-to-1 MUX is used to reduce the MOS width in each delay element [2]. In [3-4], a standard-cell based DCO is proposed. In [3], shunted tri-state buffers are used as fine-tuning of the DCO, and path selector is used as coarse-tuning of the DCO. Thus both wide operating range and high resolution can be achieved.

In this paper, an all-digital phase-locked loop for high-speed clock generation is proposed, and the ADPLL can be implemented with standard cell library. Since all circuits can be realized by standard cells, the proposed ADPLL can easily be ported to different processes in a short time. Thus the proposed ADPLL is suitable for System-On-Chip (SoC) applications since both the design time and design complexity can be reduced.

This paper is arranged as follows: Section 2 describes the proposed ADPLL architecture and frequency acquisition algorithm. The implementation of the proposed ADPLL with standard cell library in a 0.35μm 1P4M CMOS process is presented in Section 3. Section 4 shows simulation results of the proto-type chip. Section 5 concludes this paper with a summary.

2. ARCHITECUTRE OVERVIEW

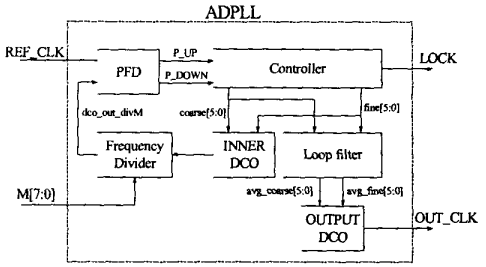

Fig.1: The proposed ADPLL block diagram

Fig. 1 shows the block diagram of the proposed ADPLL. The REF_CLK means reference clock, and M [7:0] means the division ratio between OUT_CLK and REF_CLK. The ADPLL consists of six modules namely: Phase and Frequency Detector (PFD), inner DCO, output DCO, ADPLL controller, frequency divider, and loop filter. There are two DCOs in the ADPLL, one is used for tracking the reference clock, and the other is used for generating output clock.

The signal dco_out_divM signal comes from the output of inner DCO divided by M. The PFD detects the frequency difference and phase error between REF_CLK and dco_out_divM signal. When the PFD generates P_UP signal or P_DOWN signal, it indicates the inner DCO should be speeded up or slowed down respectively. When the controller receives those signals, it will change the inner DCO's control code: coarse [5:0] and fine [5:0] to alter the inner DCO's output frequency. This inner DCO's control code is also sent to the loop filter. After ADPLL finished frequency acquisition, loop filter will detect the maximum inner DCO control code and minimum inner DCO control code during 512 reference clock cycles, then output (DCO control code $_{(max)}$ + DCO control code $_{(min)}$)/2 as the average DCO control code for the output DCO. Thus output clock will have low-jitter even with a noisy reference clock.

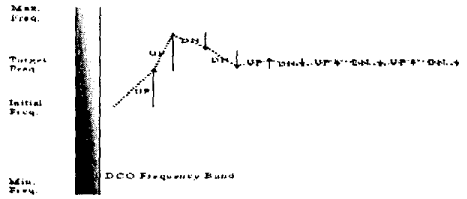

Fig. 2: Frequency acquisition of ADPLL Controller

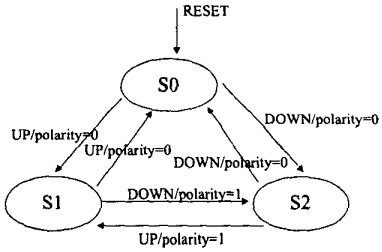

Fig.3: State diagram of the polarity detector

Fig.2 shows the frequency acquisition of the ADPLL controller. The frequency acquisition starts from the middle operating range of the DCO. When controller receives P_UP or P_DOWN signal from PFD, it will increase the DCO's output frequency or decrease the DCO's output frequency respectively. The search step for frequency acquisition is 1/4 of the DCO's operating range in the beginning. Every time when PFD's output changes from P_UP to P_DOWN or vice versa, the search step becomes reduced to one half of the previous search step. And after the search step becomes 1, the frequency acquisition is finished. Fig.3 shows the state diagram of the polarity detector used in controller, the polarity detector will find the transition of PFD's output, and send polarity change detect signal to the controller.

After frequency acquisition is finished, only DCO fine-tuning control code will be changed, and loop filter will eliminate the damping effect caused by the limitation of PFD's sensitivity and DCO's frequency resolution.

3. CIRCUIT DESCRIPTION

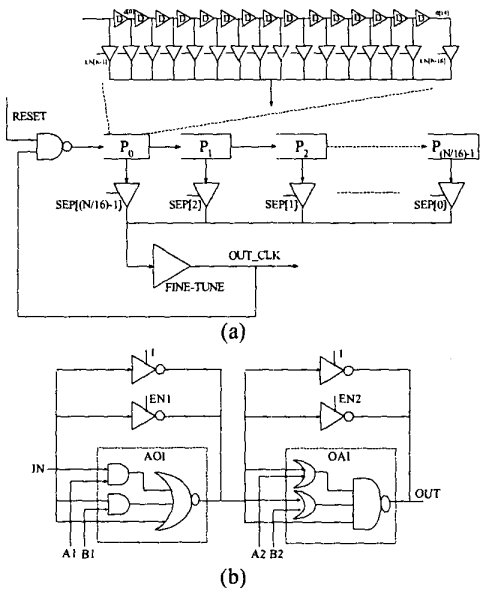

Fig.4: (a) Architecture of the proposed DCO (b) Fine-tuning delay cell

Fig. 4(a) shows the proposed architecture of the DCO. The DCO is implemented with a 0.35μm 1P4M CMOS standard cell library. It is separated into two stages: coarse-tuning stage and fine-tuning stage. In coarse-tuning stage, the 64-to-1 MUX is used to select 64 different paths. The 64-to-1 MUX is constructed by tri-state buffers. Only one path will be turned on and be selected in coarse-tuning stage. The delay time difference between two neighbor paths is determined by one coarse-tuning delay cell. The $T_{PHL} + T_{PLH}$ of one coarse-tuning delay cell is about 300ps. Thus when DCO coarse-tuning control code increases one or decreases one, the period of the output clock will be changed by ±300ps.

To increase the frequency resolution of the DCO, fine-tuning delay cell is added after coarse-tuning stage. Fine-tuning delay cell is shown in Fig.4 (b)[5]. The fine-tuning delay cell consists of And-or-invert (AOI) cell and Or-and-invert (OAI) cell. Both AOI cell and OAI cell are shunted with two tri-sate buffers. Shunted tri-state buffers can increase the controllable range of fine-tuning delay cell. And the controllable range of fine-tuning delay should cover one coarse-tuning step (i.e. 300ps). In fine-

tuning delay cell, totally six bits (EN1 A1 B1 EN2 A2 B2) can be controlled. Thus 64(=2^6) different delay steps can be used. From HSPICE simulation, the resolution of the DCO can be improved to 5ps by adding fine-tuning delay cell.

The maximum output frequency of DCO is 545MHz (1.833ns) and minimum output frequency of DCO is 41MHz (24.261ns) by HSPICE simulation.

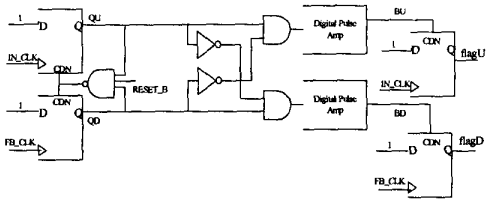

Fig.5: Phase and Frequency Detector (PFD)

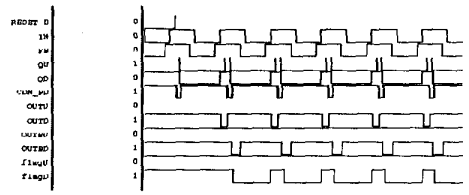

Fig.6: Simulation waveform of the PFD.

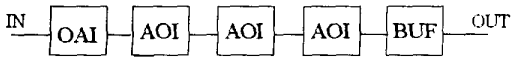

Fig. 7: Digital Pulse Amplifier

Fig.5 shows the circuit of PFD, and Fig.6 shows the simulation waveform of the PFD. When FB_CLK leads IN_CLK, flagD will generate a low pulse and flagU will remain at high. When FB_CLK legs IN_CLK, flagU will generate a low pulse and flagD will remain at high. The signal (flagU AND flagD) will be the trigger clock for the controller.

The digital pulse amplifier is shown in Fig. 7. It uses the asymmetry propagation delay between T_{PHL} and T_{PLH} in AOI cells and OAI cells to increase the pulse width of OUTU and OUTD to meet the pulse width requirement for D-Flip/Flop's reset pin. This timing requirement in 0.35μm 1P4M CMOS cell library is 800ps. The digital pulse amplifier can increase a pulse width larger than 100ps to 800ps. Thus the sensitivity of PFD can be improved to ±100ps.

ADPLL controller, frequency divider, and loop filter are described by Hardware Description Language (HDL). And they can be synthesized to gate-level circuits by logic synthesizer.

Therefore a systematic way is provided to design the ADPLL with specified standard cell library. Firstly, transistor level simulation of the fine-tuning delay cell should be done. And when the controllable range of the fine-tuning cell is determined, the suitable coarse-tuning cell whose $T_{PHL}+T_{PLH}$ is less than or equal to the controllable range of fine-tuning delay cell, can be selected from cell library. The output clock specifications determine the number of select paths in coarse-tuning stage. The rest of ADPLL are realized by logic synthesizer. Thus the design time and the complexity to design an ADPLL can be reduced. And the proposed ADPLL architecture can easily be ported to different process in a short time.

4. EXPERIMENTAL RESULTS

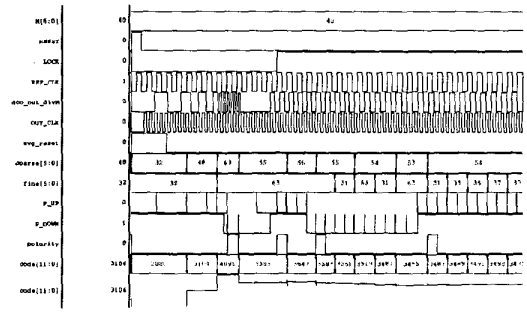

Fig.8: Post-layout simulation of the ADPLL (@200MHz)

Fig.8 shows the frequency acquisition of the ADPLL. The reference clock is 5MHz, and the division ratio M is 40. Thus the output frequency is 200MHz(=5MHz*40). When RESET=0, the ADPLL starts to work. If dco_out_divM's frequency is higher than reference clock, the PFD will generate P_DOWN signal to indicate the inner DCO should be slowed down, and when dco_out_divM's frequency is lower than reference clock, P_DOWN signal will be generated to speed up the inner DCO.

Next control code is code [11:0] + step [11:0] or code [11:0] - step [11:0], and step is 1024 in the beginning. When the polarity transition is detected from polarity detector, the search step for frequency acquisition will be reduced to one half of the previous search step. And when polarity transition happens twice, which means the upper bound and lower bound for target frequency has been determined. To further speed up the frequency acquisition process, the step will be directly reduced to 64. Thus the DCO control code: code [11:0], which means {coarse [5:0], fine [5:0]}, will be converged to the fine-tuning region in 16 reference clock cycles. And after search step is reduced to 1, the frequency acquisition is completed.

After ADPLL is locked, the loop filter will take the average of DCO control code. Fig. 9 shows the simulation waveform for the loop filter. In Fig.9, the reference clock is 7.8125MHz, and M is 64, thus the output frequency is 500MHz. When ADPLL is locked, the DCO control code

is converged to the fine-tuning region. The maximum DCO code and minimum DCO control code during 512 reference clock cycles will be almost the same. There will have a small damping in DCO control code. This damping effect in DCO control code is caused by the sensitivity limitation of the PFD and the resolution limitation of the DCO. Since the PFD has dead zone, thus when it cannot distinguish two different frequencies, the phase error will be accumulated. And when the accumulated phase error is large enough to change the polarity of PFD. The DCO control code will have a damping. Thus the loop filter will take the average of the DCO control code and output it as the avg_coarse [5:0], avg_fine [5:0] in Fig.9. In Fig.9, the avg_coarse [5:0] remains the same during average process, and only small variations in avg_fine [5:0] is found.

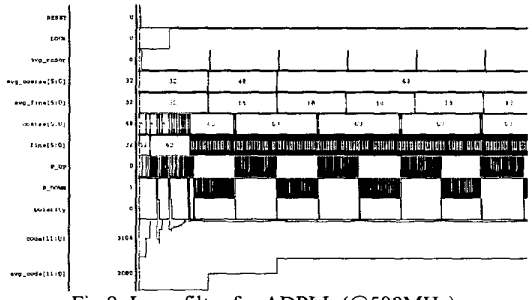

Fig.9: Loop filter for ADPLL (@500MHz)

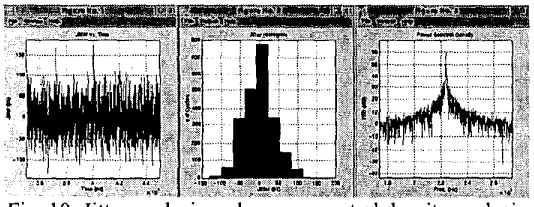

Fig. 10: Jitter analysis and power spectral density analysis for the ADPLL. (@200MHz)

Fig.10 shows the jitter analysis and power spectral density analysis for the proposed ADPLL. The jitter analysis and power spectral density analysis are calculated from the post-layout simulation waveforms during a period of 8μs. The reference clock is 10MHz (100ns), and the division ratio M is 20. It has a peak-to-peak jitter: ±1800ps and the rms jitter is 800ps. Fig. 10 shows that the peak-to-peak jitter of the output clock is ±170ps, and rms jitter of the output clock is 39ps. And phase noise of output clock is –40dBc@(100kHz). The jitter comes from reference clock can be reduced by loop filter.

Fig.11 shows the layout of the ADPLL. The layout of ADPLL is generated by Auto Placement and Routing (APR) tool. Two DCOs and the PFD should have region constraint to minimize the wire-loading effect during APR. The gate count of the ADPLL is 4800. The core size of the ADPLL is 840μm x 840μm, and the chip size including I/O pads is 2010μm x 2010μm. The power for ADPLL is 100mW(@500MHz).

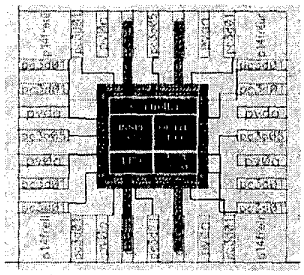

Fig.11: Layout of ADPLL

5. CONLUSION

In this paper, an all-digital phase-locked loop is presented. The ADPLL can be implemented with standard cells. And it has portability for different processes. The ADPLL implemented in a 0.35μm 1P4M CMOS standard cell library, can operate from 40MHz to 540MHz. The p-p jitter of the output clock is less than ±170ps, and the rms jitter of the output clock is less than 39ps. A systematic way to design ADPLL is also introduced. The proposed ADPLL can reduce design time and circuit complexity. Therefore it is very suitable for SoC applications.

6. REFERENCES

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