A Novel Structure for Portable Digitally Controlled Oscillator

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***Abstract*—A new structure for digitally controlled oscillator (DCO) is presented in this paper. The proposed structure of DCO is implemented by standard cell library, and with the help of C program and HSPICE simulator, the DCO can be designed in a systematic way. The DCO, which is realized on a 1P4M 0.35-μm CMOS process, has a target frequency at 250MHz, and it covers three process, voltage, and temperature (PVT) conditions: (FF, 3.6V, 0°C), (TT, 3.3V, 25°C), and (SS, 3.0V, 100° C). The DCO, which is realized on a 1P5M 0.25-μm CMOS process, has a target frequency at 400MHz, and it covers three PVT conditions: (FF, 2.75V, 0°C), (TT, 2.5V, 25°C), and (SS, 2.25V, 100°C). The DCO has 32-bit control and achieves LSB resolution under 1ps.**

I. INTRODUCTION

THE all-digital phase-locked loops (ADPLL's) became more and more popular in recently years. The digital nature of the ADPLL's makes it possible to achieve very fast lock times. Fig. 1 shows the ADPLL's block diagram. The major concept is used as an oscillator to lock or track input signals in both phase and frequency [1]. In the core of the ADPLL's is the Digitally-Controlled Oscillator (DCO). The resolution of the DCO determines the phase error and frequency mismatch of the ADPLL's, and the operating range of the DCO limits the ADPLL's pulling range.

Like most voltage-controlled oscillator, the DCO also has the frequency control mechanism within an oscillator block. There are two parameters to modulate the output frequency of the ring oscillator. One is the propagation delay time of each delay cell, and the other is the total number of the delay cells in the closed loop. Many structures had been built to improve the operating bandwidth and resolution of the DCO [2-5]. In [2], two structures are used to meet this goal; one is path selector, and the other is delay matrix. Path selector changes the total number of the delay cells in the closed loop thus increases dynamic controlled range coarsely. Parallel tri-state buffers used in delay matrix alter the driving ability of the inverter, and thus change the DCO's output frequency finely. In [3-5], similar architecture are used expect for the delay cell is constructed by the binary weighted MOS switches.

For some applications, the ADPLL's does not need to generate multiple frequencies, and only needs to generate one specified frequency. In those applications, the DCO doesn't need to have large pulling range, but the target frequency must be covered in all possible operating conditions. That means the process variations, temperature variations, and voltage variations (PVT effects) must both be considered carefully.

This work was supported by the National Science Council of Taiwan, R.O.C., under Grant NSC89-2215-E-009-053.

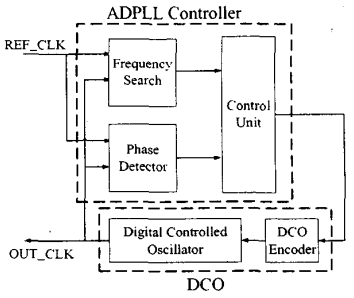

Fig. 1. ADPLL block diagram.

This paper describes a novel structure for portable DCO. Based on the proposed structure, portable cell-based implementations for DCO are completed by standard cell. The DCO, which is realized on a 1P4M 0.35-μm CMOS process, has a target frequency at 250MHz, and it covers three PVT conditions: (FF, 3.6V, 0°C), (TT, 3.3V, 25°C), and (SS, 3.0V, 100°C), and it can operate from 150MHz to 420MHz in typical case. The DCO, which is realized on a 1P5M 0.25-μm CMOS process, has a target frequency at 400MHz, and it covers three PVT conditions: (FF, 2.75V, 0°C), (TT, 2.5V, 25°C), and (SS, 2.25V, 100°C), and it can operate from 170MHz to 650MHz in typical case. With the timing calibration data of each delay cell, which was simulated from the HSPICE, and the help of the C programs, DCO can be designed in a systematic way. The reset of this paper is organized as follows. The proposed architecture of the DCO is introduced in Section II. The implementations for DCO with 0.35-μm and 0.25-μm CMOS standard cells are described in Section III. The C program simulation results, the compared HSPICE simulation results, and the measured results from IC chip, are also presented in Section III. Section IV gives some conclusions.

II. THE PROPOSED DIGITALLY CONTROLLED OSCILLATOR

The basic element in the DCO is the variable delay inverter. In [3-5], the width of MOS switches are binary weighted and MOS switches are used to change the equivalent MOS width of pull-up or pull-down path. As the digital control word changes, propagation delay time of the inverter will trend to be inversely proportional to the equivalent MOS width.

In standard cell library, there are many cells having this same behavior, such as AND-OR cells or OR-AND cells. Fig. 2 shows the schematic of the AND-OR 222 cell, and the corresponding static CMOS circuit. If A1, B1, C1, and C2 in Fig. 2(a) are connected to signal "VC", A2 is connected to signal "VA", and

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B2 is connected to signal "VB". The truth table of this cell is listed in table I, and in any combination of (VA, VB) inputs, ZN is still the logic inverse of VC.

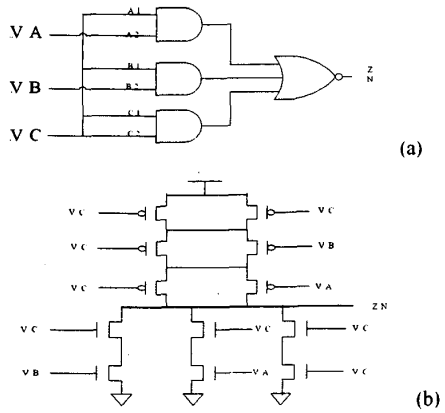


Fig. 2. (a) Schematic of AOI 222 (b)CMOS circuit of AOI 222

When (VA, VB) is equal to (1,1), the T_{PHL} from VC to ZN is less than (VA, VB)=(0,1) or (1,0). In the other case of (VA, VB)=(1,0) or (0,1), the T_{PHL} from VC to ZN is less than (VA, VB)=(0,0). This is result from the change of the equivalent MOS width in pull-down path. Thus this cell becomes a delay-controllable inverter and will have four different propagation delay time.

Furthermore, the controllable range of this inverter can be improved. Fig. 3 shows the improved architecture of the delay cell. Parallel tri-state buffers are used to increase the bandwidth of the inverter. Finally, each variable delay inverter will have n+2 control bit and 4*(n+1) different propagation delays.

Fig. 4(a) shows the proposed digitally controlled oscillator, this ring oscillator has m+1 stages and one reset stage, each stage has (n+2)-bit controls, and totally (m+1)(n+2)-bit controls are needed. The summation of propagation delay in each delay cell determines the DCO's output frequency. Ideally, the total output frequencies are $[4(n+1)]^{(m+1)}$. But there are some limitations make it impossible, such as the area constraint of the DCO encoder, and in some control commands, the difference of DCO's output signals are too small to be distinguished. The schematic of the reset stage is shown in Fig. 4(b). The reset stage is needed in the startup phase of the ADPLL to make sure that the ring oscillator will oscillate. The input capacitance of VC is maintained the same compared to the delay cell.

III. THE IMPLEMENTAION OF DCO AND SIMULATION RESULT

The propagation delay time of each delay cell for 0.35-μm and 0.25-μm CMOS process is simulated by HSPICE, and is listed in table II. Each delay cell has two parallel tri-state buffers, thus each delay cell has twelve different propagation delays. The period of the DCO's output signal equals

$$T_{period} = \sum T_{ij} \qquad (1)$$

where T_{ij} means the propagation delay time of the i-th stage with the specified control j.

TABLE I

TRUE TABLE OF VARIABLE DELAY CELL

VC	VA	VB	ZN
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

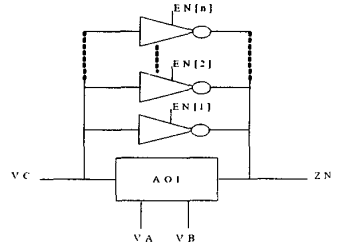
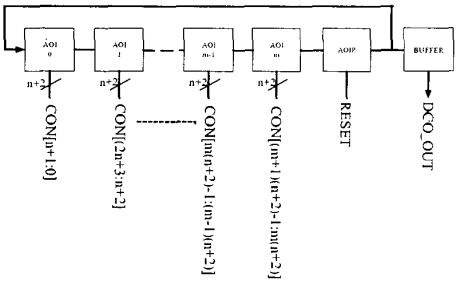


Fig. 3. The improved delay cell

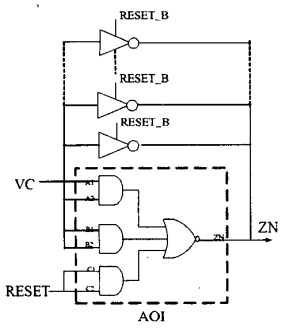
When target frequency is specified, the number of delay cells can be determined from the timing data that are listed in table II.

Fig. 5 shows the HSPICE simulation results of the 250MHz DCO on a 0.35-μm CMOS process. The 250MHz DCO has eight delay cells, and each delay cell has two parallel tri-state buffers, (m, n)=(7, 2). It can operate from 150MHz to 420MHz in typical case. The compared operating range of the DCO in three PVT conditions: (FF, 3.6V, 0°C), (TT, 3.3V 25°C), and (SS, 3.0V, 100°C) are also shown in Fig. 5. From the simulation results, the target frequency 250MHz is covered in different PVT conditions. The power consumption at output frequency 250MHz is 13.9mW.

Fig. 6 shows the HSPICE simulation results of the 400MHz DCO on a 0.25-μm CMOS process. The 400MHz DCO has eight delay cells, and each delay cell has two parallel tri-state buffers, (m, n)=(7, 2). It can operate from 170MHz to 650MHz in typical case. The compared operating range of the DCO in three PVT conditions: (FF, 2.75V, 0°C), (TT, 2.5V, 25°C), and (SS, 2.25V, 100°C) are also shown in Fig. 6. From simulation results, the target frequency 400MHz is covered in different PVT conditions. The power consumption at output frequency 400MHz is 2.6mW.



(a)



(b)

Fig. 4. (a)The proposed architecture of the DCO. (b) Schematic of the RESET stage

The output frequency of the DCO with specified control command can be calculated by C program. Fig. 7 shows the cell library calibration model. The current delay cell has twelve states, and the next delay cell also has twelve states. The rise time and fall time of the previous stage varies from 0.1ns to 1.2ns (step 0.1ns). Using HSPICE to calculate T_{PHL} and T_{PLH} of the current stage in each possible case (12*12*12*12) and creates a lookup table. Then the output frequency with specific control command can be calculated by summation of the T_{PHL} and T_{PLH} in each delay cell. In this calibration model, rise time and fall time of the previous stage is considered, and the output loading variations (including current stage's output capacitance and next stage's input capacitance) are also considered. Thus the periods of the DCO's output clock, which have 1ps difference, can be calculated from the C program. To make sure the output frequency calculated by C program correspond to HSPICE simulation result, the delay cell shall be designed to minimize the output rise time and fall time, so that the equation 1 can still work. If the rise time and fall time of each delay cell is too slow, the equation 1 will not accuracy. This is because the slowly rise time and fall time will increase the next stage's propagation delay.

TABLE II

PROPAGATION DELAY OF EACH DELAY CELL (T_{ij})

	CONTROL				$T_{PHL}+T_{PLH}$ (0.35-μm)	$T_{PHL}+T_{PLH}$ (0.25-μm)
	EN2	EN1	VA	VB	Time unit: (0.1ns)	Time unit: (0.1ns)
j=0	0	0	0	0	6.53038	5.01584
j=1	0	0	0	1	5.81441	3.65654
j=2	0	0	1	0	4.52679	3.14126
j=3	0	0	1	1	4.95071	3.22097
j=4	0	1	0	0	3.78074	2.31819
j=5	0	1	0	1	3.34552	2.00708
j=6	0	1	1	0	2.76979	1.79185
j=7	0	1	1	1	2.75505	1.73833
j=8	1	1	0	0	2.91896	1.71033
j=9	1	1	0	1	2.63420	1.55570
j=10	1	1	1	0	2.25919	1.42016
j=11	1	1	1	1	2.21983	1.38480

Once the lookup table was created, the DCO with specified target frequency can be designed in a systematic way. First, the stage number of the DCO can be determined from the information in table II. Second, the output frequency with specified control command can be calculated by C program. The C program can calculate output frequencies of all possible control commands. As given the constraint of minimum resolution of the DCO, the DCO encoder table can be generated by C program (selects what control command is needed from all possible cases). Third, since the DCO consists of standard cells, the layout of the DCO can be easily generated by Auto P&R tools. But when placed and routing the layout of the DCO, there need to has some region constraints to make sure the wire-load effect will not influence the performance of the DCO. Fig. 8 shows the chip layout of the 250MHz DCO and 320MHz DCO on a 1P4M 0.35-μm CMOS process. Because the IO pad has speed limitations, the output clock comes from DCO output will divided by 4, then send to the output IO pad.

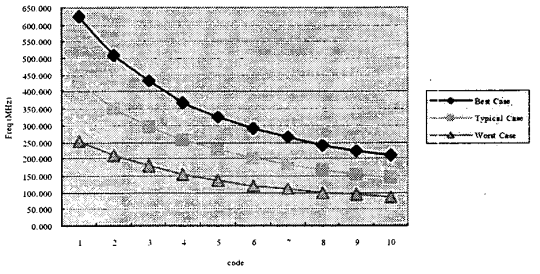


Fig. 5. Operating bandwidth in three PVT conditions. (0.35-μm)

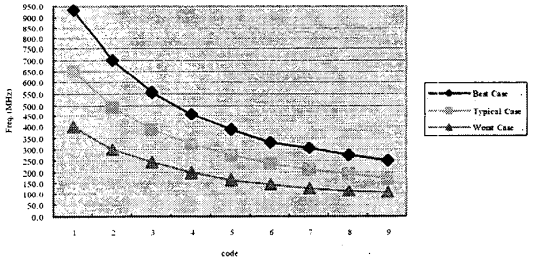


Fig. 6. Operating bandwidth in three PVT conditions. (0.25-μm)

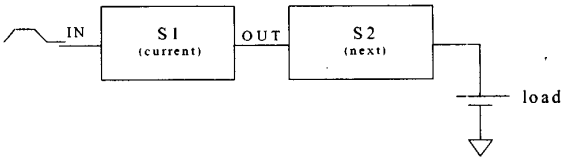


Fig. 7. Cell Library calibration model

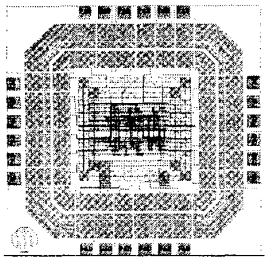


Fig.8. Chip layout of the DCO

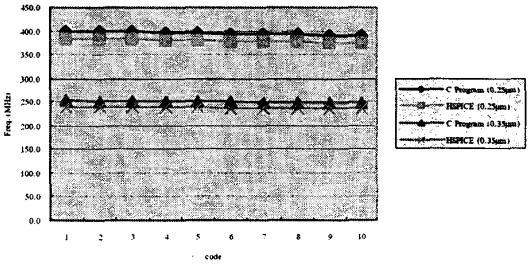


Fig. 9. Comparisons of C program results and HSPICE results

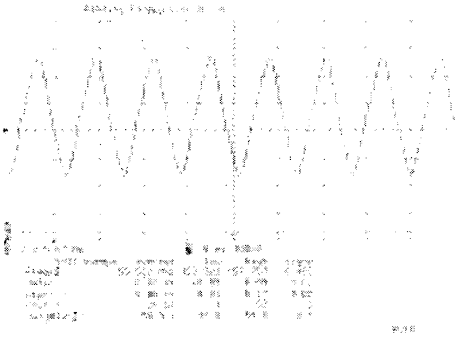


Fig. 10. Divided by 4 output clock (DCO @ 620MHz)

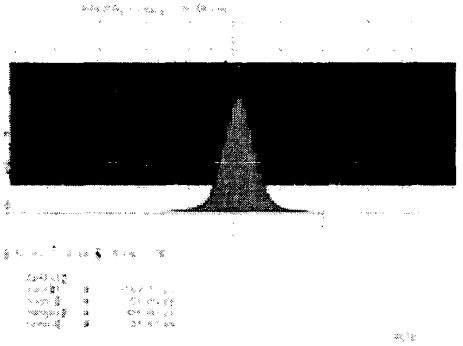


Fig.11. Histogram of long term jitter (DCO @620MHz)

In Fig. 9, C program results and HSPICE simulation results are compared in a narrow band. The absolute value of the C program result has some mismatch compared with HSPICE, but the relative differences of periods are still the same with HSPICE simulation results. The offsets between C program and HSPICE calculated results usually come from the reset stage and output buffer delay, which is not considered in the C program calculations, and will not influence the DCO's resolution. Fig.10&Fig.11 shows the measured waveforms from the chip of DCO. At 620MHz, the peak-to-peak output clock jitter of the DCO is 324ps and the rms jitter is 24.6ps. Fig.12 shows the comparisons of the C program and results measured from chip.

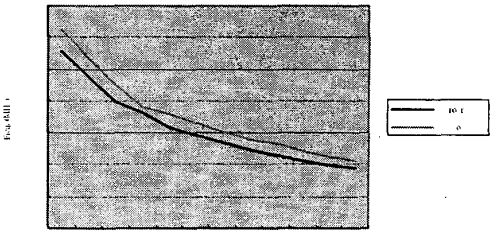


Fig.12. Comparisons of C program results and chip results

IV. CONCLUSION

The DCO, which is proposed in this paper, can be implemented by standard cells. This DCO has enough operating bandwidth to overcome different PVT conditions and to make sure that the target frequency can be covered in those conditions. When the lookup table is created by HSPICE, the design of DCO can be realized in a systematic way. The proposed DCO can be applied to ADPLL design, and can be easily ported to any process by standard cell library.

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