

An All-Digital and Wide-Range Reference Clock Generator for Biotelemetry Applications

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ABSTRACT

In this paper, an all-digital and low-power reference clock generator with cell-based design for biotelemetry applications is presented. The proposed clock generator employs a cascade-stage structure to achieve high resolution and wide range at the same time. Besides, based on the proposed Schmitt-trigger-based delay cell (STDC), hysteresis delay cell (HDC), and digitally controlled varactor (DCV), the proposed clock generator not only can provide high resolution, but also can generate low frequency clock signal with low power consumption and low circuit complexity as compared with conventional approaches. Simulation results show that the operation frequency range is from 9.9MHz to 823MHz, and the power consumption can be improved to 114 μ W (@10MHz) with 6.42ps resolution. In addition, the proposed clock generator can be implemented with standard cells, making it easily portable to different processes and very suitable for biomedical System-On-Chip (SoC) applications.

KEYWORDS

WBAN, DCO, SoC, PLL, All Digital, Low Power.

1 INTRODUCTION

As the wireless communication and integrated circuit (IC) technology develop rapidly, the medical services extend from the closed in-hospital systems to any open roaming spaces. Through the wireless communication, the physiological information of patient that

provided by the wearable or implantable devices in the body can send to the hospital for healthcare and health monitoring immediately. Figure 1 illustrates the concept of wireless healthcare and health monitoring system. The physiological signals including electrocardiography (ECG), electroencephalogram (EEG), and temperature transmits to the personal server, such as a smart phone, by wireless body area network (WBAN), and then delivers it to the hospital or medical server by wireless networking [1], [2]. Recently, there is a large of demand in biotelemetry application; the standard of WBAN was defined in [3].

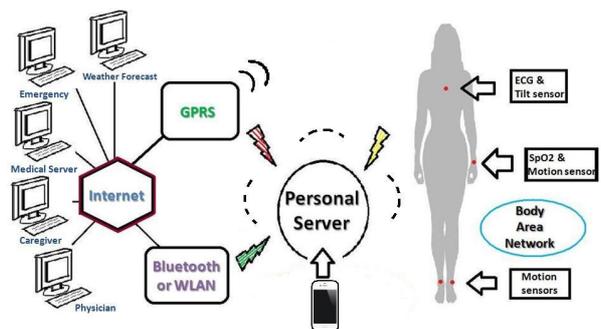


Figure 1. Concept of wireless healthcare and health monitoring system.

A typical WBAN system is shown in Figure 2. Generally, a WBAN system consists of a multiple of wireless sensor nodes (WSNs) and a central processing node (CPN). The physiological signals are sensed, filtered, and stored in these WSN, and WSN transmits the

body data wirelessly to a CPN for further processing and other applications. According to the requirements of the healthcare and health monitoring, there are several important design considerations in WBAN system [4]: First, because the electrical power of implanted devices is provided by a battery which is not replaceable and rechargeable, in order to achieve long duration monitoring for biotelemetry applications, the WSN should have an ultra-low power operation [5]. Second, as the medical devices implanted into body, the size should be as small as possible for comfortable purposes. Thus, the components should be integrated into a single chip to reduce the device size. The electronic hardware design style of WBAN moves from system-on-board (SoB) to system-on-chip (SoC). In addition, the circuit complexity of the implanted chip should be reduced to shrink the overall device area. Finally, the WBAN is required to provide reliable signal transmission for accurate healthcare and monitoring. Thus, especially in WSN, the quality of system clock source is very important.

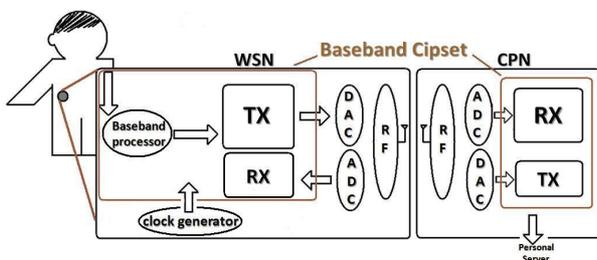


Figure 2. Architecture of WBAN system.

The WSN design usually utilizes the power management with sleep/wakeup scheme to reduce the redundant power consumption [6]. However, the system still consumes power when it moves from sleep to wakeup status. Besides, long settling time degrades the overall system performance. Thus, how to reduce the settling time of WSN is an important design consideration. Traditionally, the reference clock of WSN is provided by a quartz crystal. The frequency synthesizer, such as a phase-locked

loop (PLL), receives the reference clock from an off-chip crystal, and then generates the system clock signal with the desired frequency for WSN system. Generally, the output clock frequency range of a quartz crystal is from thousands Hz to several MHz. Based on these frequency range, the settling time of PLL is $100\mu\text{s}$ even 1ms [7], [8]. It can increase reference clock frequency to reduce the settling time of PLL to meet the system requirements [8]. However, as the reference clock frequency increases, it not only increases the power consumption of PLL, but also reduces the input noise immunity. In addition to the settling time issue, the size of quartz crystal is too large and hard to integrate into SoC, it is not suitable for the WSN in WBAN applications. Recently, a digitally controlled oscillator (DCO) as an all-digital reference clock generator for WBAN applications has been proposed [6], [9]-[11]. The output clock frequency of DCO is controlled by the digital control code. If a DCO replaces a quartz crystal as a reference clock generator, it can integrate into WSN easily; resulting in overall device size shrinking and hardware cost reduction. Although the DCO is suitable for biotelemetry applications, it still needs to further reduce power consumption, increase delay resolution, and extend frequency range.

In this paper, a high-resolution, wide-range and low-power clock generator is proposed for biotelemetry applications. The proposed DCO employs a cascade-stage structure to achieve high resolution and wide frequency range at the same time. Besides, based on the proposed cyclic-controlled delay stage (CCDS), the proposed DCO not only can achieve low-frequency output, but also have low circuit complexity and power consumption as compared with conventional approaches. In addition, the proposed DCO architecture not only can be implemented by all-digital CMOS design manner for cost and power reduction, but also can be described by hardware description language (HDL) and implemented with standard cells, making it easily portable to

different processes and very suitable for biomedical chip applications and system integration.

2 DIGITALLY CONTROLLED OSCILLATOR OVERVIEW

The design for realizing clock generator can be partitioned into analog and all-digital design approaches. Traditionally, the clock generators are realized by analog approach. However, as supply voltage decreases, both gain and frequency range need to be traded off in voltage-controlled oscillator (VCO) which is the most important block in analog clock generator. In addition, due to serious leakage current problem, it is hard to design a charge-pump circuit that is the essential block in analog clock generator in more advanced process technology. Thus it needs more design efforts to integrate analog clock generators in SoC with lower supply voltage and advanced process. Moreover, because the analog clock generator employs the passive components such as resistor and capacitor to form the loop filter, it induces large area and cost. Furthermore, as technology migrates, the analog blocks in clock generator need to be re-designed, leading to enlarge the design turn around time. In contrast to analog clock generator, a DCO uses an all-digital design approach does not utilize any passive components and use digital design approaches, making it easily be integrated into digital and low-supply voltage systems. Because all-digital clock generator is reusable as a soft intellectual property (IP), it can decrease time-to-market for a design and be very suitable for SoC applications as well as system-level integration.

Recently, different architectural solutions have been proposed to implement the DCO. The current-starved type DCO [12] controls the supply current of delay cell to obtain different delay values. Although it has high resolution, it needs a static current source that will consume more static power dissipation. The LC tank DCO [13] can also achieve high delay

resolution, however, it needs advanced process and requires intensive circuit layout. These approaches demand high complexity at circuit level, resulting in long design cycle and low portability.

In order to reduce design cycle when process or specification is changed, many DCO's implemented with standard cells have been proposed to enhance portability [14]-[16]. Driving capability modulation (DCM) changes the driving current of each delay cell by controlling number of enabled tri-state buffers/inverters [14]. The design concept of this approach is straightforward, but it has a poor performance in linearity and power consumption, and the resolution is insufficient. The or-and-inverter (OAI) cells are proposed to enhance resolution by different input pattern combinations; however linearity remains to be solved [15]. Although digitally controlled varactor (DCV) has a good performance in resolution and linearity [16], it is hard to take a few cells to provide wider operation range. As a result, large power consumption is demanded due to many DCV cells to maintain an acceptable operation range. As the mentioned above, the existed DCO architecture is not suitable for biotelemetry applications. Thus, the research target of this paper is to propose a digitally controlled oscillator (DCO) as an all-digital reference clock generator in WSN. According to the system requirements of WBAN, the proposed DCO should achieve the following features: low-frequency clock output, low power consumption, wide frequency range, high delay resolution, low circuit complexity, and high portability.

3 PROPOSED DIGITALLY CONTROLLED OSCILLATOR DESIGN

3.1 Architecture

Figure 3 illustrates the architecture of the proposed DCO which consists of a cyclic-controlled delay stage, a coarse-tuning stage (CTS), and two fine-tuning stages (FTSs). To

preserve the control code resolution and operation range, the proposed DCO employs a cascading structure to maintain control code resolution and extend operation range easily. Because the requested lowest output frequency in the system is 10MHz, the conventional delay line structure is not suitable for this application. Thus, the proposed DCO employs a CCDS to generate a low-frequency clock with a low hardware cost [17]. The CCDS is composed of a Schmitt-trigger-based delay cell (STDC), a multiplexer, a de-multiplexer, a control unit, and a flip-flop. The multiplexer and de-multiplexer will determine whether or not the DCO bypasses the inner loop. When the clock propagates through the inner loop, the control unit receives COUNT from CCDS, and then the counter in control unit adds one. When the counting results of control unit is equal to cyclic-controlled code (C1[9:0]), the delay path will change from the inner loop to outer loop. Because the period of the output clock can be easily enlarged by the cycle control code extension, the proposed DCO could achieve a wide operating frequency range. Finally, because the resolution of the CCDS is not sufficient for typical DCO applications, a CTS and two FTSs are added to further improve overall delay resolution of DCO.

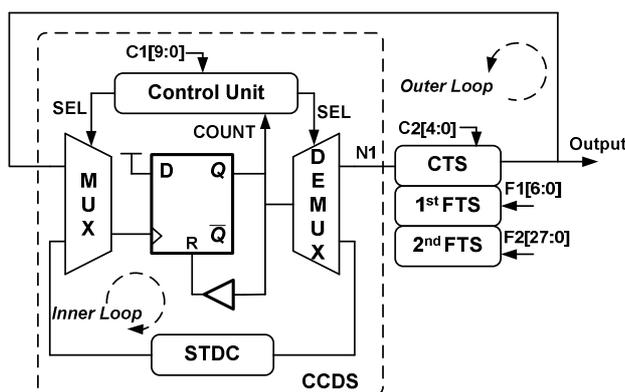


Figure 3. Block diagram of the proposed DCO.

3.2 Circuit Implementation

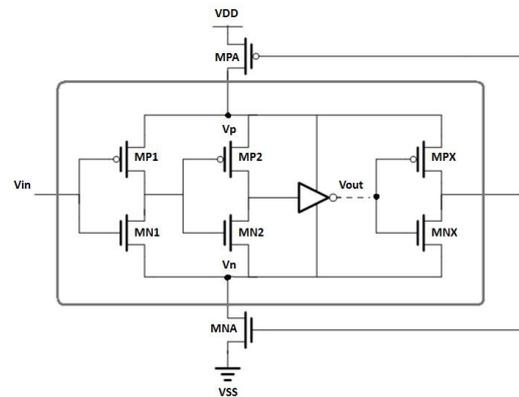


Figure 4. STDC circuit.

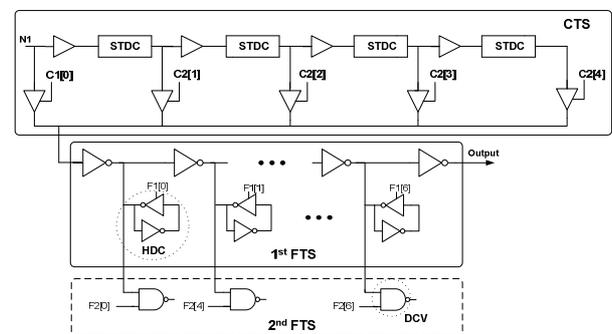


Figure 5. Circuit diagram of CTS, 1st FTS, and 2nd FTS.

Figure 4 illustrates the circuit of STDC. The Boolean function of STDC is the same as that of a normal inverter, except that HDCs have the hysteresis property induced by a Schmitt trigger [6]. Because the STDC can provide larger delay as compared with the conventional delay cell, it can replace numbers of delay cell leading to reduce power consumption and chip area. Figure 5 shows the circuit of the coarse-tuning and fine-tuning stages. There are 5 different delay paths in the CTS and only one path is selected by the path selector tri-state buffer controlled by coarse delay control code (C2[4:0]). The delay of 1st and 2nd FTS is controlled by fine delay control F1[6:0] and F2[6:0], respectively. The 1st FTS is composed of 7 hysteresis delay cells (HDC), and each of which contains one inverter and one tri-state inverter. When the tri-state inverter in HDC is enabled, the output signal of enabled tri-state inverter has the hysteresis phenomenon to

increase delay [16]. The digitally controlled varactors (DCV's) are exploited in the 2nd FTS to further improve the overall resolution of DCO. The operation concept of DCV is to control the gate capacitance of logic gate with enable signal state to adjust the delay time [16].

4 EXPERIMENTAL RESULTS

The proposed DCO is designed and implemented by 90nm 1P9M CMOS standard cell library and cell-based design flow, where the DCO HSPICE simulation results of controllable delay range and the finest delay step of different tuning stages in the typical case (TT, 1.0V, 25°C), the best case (FF, 1.1V, 0°C), and the worst case (SS, 0.9V, 85°C) are shown in Table I. Because the finest step of 2nd FTS determines the DCO resolution, the proposed DCO can achieve high resolution with 6.42ps. It should be noted that the controllable delay range of each stage is larger than the finest delay step of the previous stage. As a result, the cascading DCO structure does not have any dead zone larger than the LSB resolution of DCO. The code-to-delay simulation results of different tuning stages are shown in Figure 6. The operation frequency range is from 9.9MHz to 823MHz, and the power consumption can be improved to 114μW and 310μW at 10MHz and 823MHz, respectively. The performance summary is listed in Table II.

Table 1. Simulation results of step/range of tuning ranges

	Best Case		Typical Case		Worst Case	
	Step (ps)	Range(ps)	Step (ps)	Range(ps)	Step (ps)	Range(ps)
CCDS	607.15		1214.6		2189.9	
CTS	155.65	622.67	269.99	1231.4	494.58	2623.5
1 st FTS	23.06	161.58	44.68	310.57	76.94	508.59
2 nd FTS	3.92	28.48	6.42	47.28	11.94	84.96

5 CONCLUSION

In this paper, we have proposed a high-resolution and wide-range, and low-power

DCO with cell-based design for biotelemetry applications. The proposed DCO employs a cascade-stage structure including CCDS, CTS, and FTS to achieve high timing resolution and wide frequency range at the same time. Besides, based on the STDC, HDC, and DCV, the proposed clock generator can generate low frequency clock signal with low power consumption and low circuit complexity as compared with conventional approaches. Moreover, because the proposed DCO has a good portability as a soft intellectual property (IP), it can reduce both design time and complexity. As a result, it is very suitable for System-on-Chip (SoC) applications as well as system-level integration.

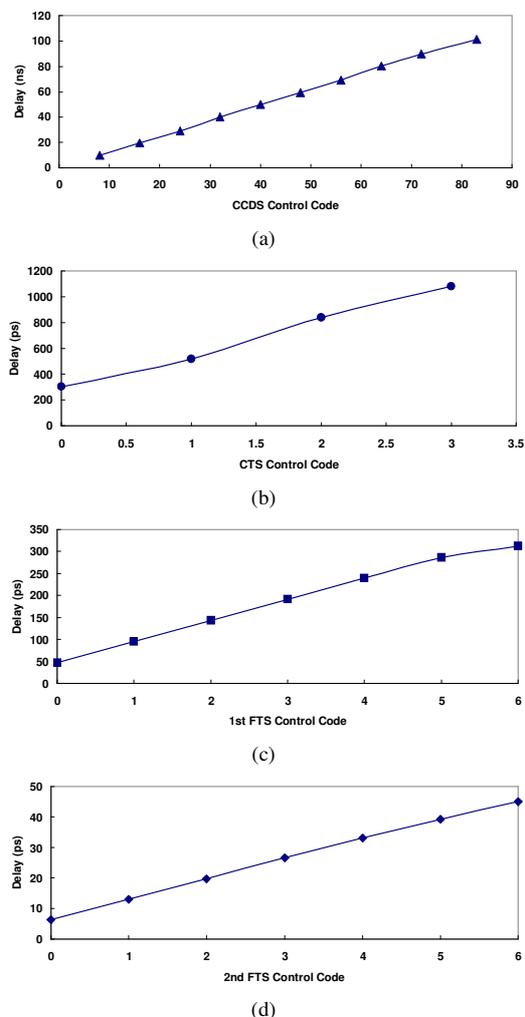


Figure 6. Simulation results of (a) CCDS, (b) CTS, (c) 1st FTS, and (d) 2nd FTS.

Table 2. Performance Summary

Performance Indices	Proposed DCO
Process	90nm CMOS
Operation Range (MHz)	9.9 ~ 823
LSB Resolution (ps)	6.42
Power Consumption (mW)	0.114@10MHz 0.310@823MHz
Portability	Yes

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REFERENCES

- [1] C. A. Otto, E. Jovanov, and A. Milenkovic, "A WBAN-based system for health monitoring at home," *Proceedings of the 3rd IEEE-EMBS International Summer School and Symposium on Medical Devices and Biosensors*, Sep. 2006, pp. 20-23.
- [2] T. -W. Chen, J.-Y. Yu, C. -Y. Yu, and C. -Y. Lee, "A 0.5 V 4.85 Mbps dual-mode baseband transceiver with extended frequency calibration for biotelemetry applications," *IEEE J. of Solid-State Circuits*, vol. 44, pp. 2966-2976, Nov. 2009.
- [3] Body Area Networks (BAN), IEEE 802.15 WPAN Task Group 6, Nov. 2007. [Online]. Available: <http://www.ieee802.org/15/pub/TG6.html>.
- [4] W. -H. Sung, J. -Y. Yu, and C. -Y. Lee, "A robust frequency tracking loop for energy-efficient crystal-less WBAN systems," *IEEE Trans. Circuits and Syst. II, Express Briefs*, vol. 58, no. 10, pp. 367-364, Oct. 2011.
- [5] H. Lhermet, C. Condemine, M. Plissonnier, R. Salot, P. Audebert, and M. Rosset, "Efficient power management circuit: Thermal energy harvesting to above-IC microbattery energy storage," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2007, pp. 62-63.
- [6] S. -Y. Hsu, J. -Y. Yu, and C. -Y. Lee, "A sub-10- μ W digitally controlled oscillator based on hysteresis delay cell topologies for WBAN applications," *IEEE Trans. Circuits Syst. II*, vol.57, no.12, pp.951-955, Dec. 2010.
- [7] P. Choi, H. C. Park, S. Kim, S. Park, I. Nam, T. W. Kim, S. Park, S. Shin, M. S. Kim, K. Kang, Y. Ku, H. Choi, S. Min Park, and K. Lee, "An experimental coin-sized radio for extremely low-power WPAN (IEEE 802.15.4) application at 2.4GHz," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2258-2268, Dec. 2003.
- [8] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ: Prentice-Hall, 1998.
- [9] Y. Tokunaga, S. Sakiyama, A. Matsumoto, and S. Doshio, "An on-chip CMOS relaxation oscillator with power averaging feedback using a reference proportional to supply voltage," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2009, pp. 404-405.
- [10] C. -Y. Yu, J. -Y. Yu, and C. -Y. Lee, "An eCrystal oscillator with self-calibration capability," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2009, pp. 237-240.
- [11] W. -H. Sung, S. -Y. Hsu, J. -Y. Yu, C. -Y. Yu, and C. -Y. Lee, "A frequency accuracy enhanced sub-10- μ W on-chip clock generator for energy efficient crystal-less wireless biotelemetry applications," in *Proc. IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2010, pp. 115-116.
- [12] J. Dunning, G. Garcia, J. Lundberg, and E. Nuckolls, "An all-digital phase-locked loop with 50-cycle lock time suitable for high-performance microprocessors," *IEEE J. Solid-State Circuits*, vol. 30, pp. 412-422, Apr. 1995.
- [13] R. B. Staszewski, D. Leipold, K. Muhammad, and P. T. Balsara, "Digitally controlled oscillator (DCO)-based architecture for RF frequency synthesis in a deep-submicrometer CMOS process," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process*, vol. 50, no. 11, pp. 815-828, Nov. 2003.
- [14] T. Olsson and P. Nilsson, "A digitally controlled PLL for Soc applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 751-760, May. 2004.
- [15] C. -C. Chung and C. -Y. Lee, "An all digital phase-locked loop for high-speed clock generation," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 347-351, Feb. 2003.
- [16] D. Sheng, C. -C. Chung and C. -Y. Lee, "An ultra-low-power and portable digitally controlled oscillator for SoC applications," *IEEE Trans. Circuits and Syst. II, Exp. Briefs*, vol. 54, no. 11, pp. 954-958, Nov. 2007.
- [17] C. -C. Chung, D. Sheng, C. -L. Chang, W. -D. Ho, Y. -D. Lin, and F. -N. Lu, "An all-digital large-N audio frequency synthesizer for HDMI applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 7, pp. 424-428, Jul. 2012.