An FPGA-based Transceiver for Human Body Channel Communication using Walsh Codes

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***Abstract*-- In this paper, a body channel communication (BCC) transceiver with Walsh codes modulation is presented. In the transmitter part, data are encoded in Walsh code format, and the chosen Walsh codes restrict the maximum consecutive identical digit (CID) to increase the data transitions. In the receiver part, we use an analog front-end (AFE) circuit board to amplify the attenuated signal from the transmitter and restore the signal to the digital waveform. After the 8x oversampling sampler and vote integrator recovery the clock and data, the Walsh code demodulator demodulates the original data. The proposed BCC transceiver has higher data reliability because of the orthogonal characteristic of Walsh codes. Moreover, the proposed Walsh code concatenated method strengthens the jitter tolerance and improve the code rate. The proposed BCC transceiver was verified on a field-programmable gate array (FPGA) board. The chip rate of the proposed transceiver ranges from 1.56 Mcps to 12.5 Mcps. Also, the bit error rate is < 10^{-8} and < 10^{-5} at 6.25 Mcps and 12.5 Mcps, respectively.**

I. INTRODUCTION

Recently, healthcare devices and consumer electronics are more and more popular, and wireless body area network (WBAN) is usually utilized to implement above applications. In wireless communication, Bluetooth, ZigBee, and Radio Frequency Identification (RFID) are well-known techniques. The low data rate, large power consumption are problems on wireless communication. Moreover, the RF transmission has many interferences in the environment. Body channel communication (BCC) utilizes human body as a communication medium to transmit data. It has characterizations of a high data rate and relatively low power consumption [1-5]. The BCC technology can overcome problems of wireless communication.

In [1, 4], a wide-band signaling (WBS) scheme is adopted in the design of the BCC transceiver. Jitter accumulation and duty-cycle distortion happen when the signal transmits through a human body. This situation increases the difficulty in recovering data in the receiver part. In [2], a frequency-shift keying (FSK) modulation scheme is adopted. The frequencies of the FSK should be chosen carefully to avoid the popular frequency bands. The other drawback is the active filters required in the dual-band receiver occupied a large chip area. In [3], an orthogonal frequency-division multiplexing (OFDM) BCC transceiver has been proposed. Although the OFDM-based transceiver can enhance the data rate, there is also high power consumption and occupies large chip area.

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In this paper, an FPGA-based BCC transceiver is presented. In the transceiver, the adopted Walsh code modulation approach can enhance the data reliability. Moreover, the concatenated method can enhance peak to peak jitter tolerance to 25ns at 12.5Mcps with four 4-bit Walsh codes concatenated.

II. PROPOSED ARCHITECTURE

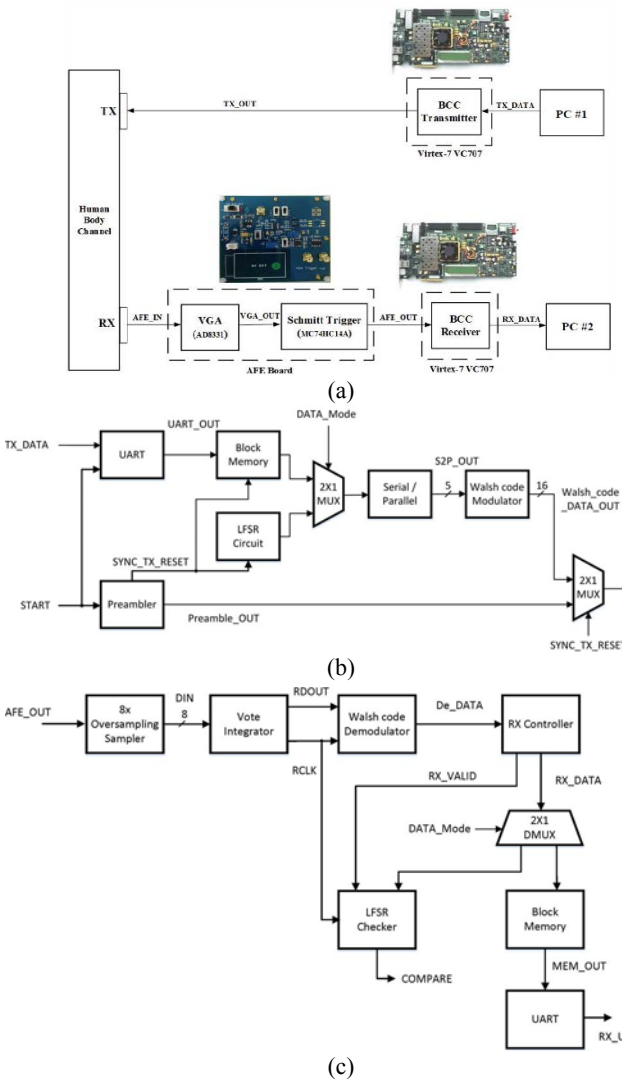

Fig. 1 (a) Proposed FPGA-based BCC transceiver (b) Transmitter (c) Receiver.

The architecture of the proposed FPGA-based transceiver is shown in Fig. 1(a). The transceiver consists of a transmitter (TX), a receiver (RX), and an analog frontend (AFE) circuit. First, the PC #1 sends the media data to the block memory of the TX FPGA through the UART interface. After the media data stored ready and are modulated with Walsh codes, the

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data will pass through the human body channel to an AFE board to amplify the attenuated signal. Then, the RX FPGA board with an 8x oversampling clock and data recovery (CDR) circuit to restore the clock and data. Subsequently, the Walsh code demodulator demodulates data to the original data. Finally. The RX FPGA sends the received data to the PC #2 to display the media data.

The BCC transmitter shown in Fig. 1(b) has two modes. In random data mode, the LFSR circuit generates the random data for the transmitter. In media data mode, image data from PC #1 are stored in the TX FPGA and then sent to the human body channel. The chosen sets of Walsh code limit the maximum continuous identical digits (CID).

In the proposed BCC receiver shown in Fig. 1(c), the 8x oversampling sampler and vote integrator is used to recover the clock and data. The 8x oversampling sampler samples eight data at one symbol period. The vote integrator uses these data to determine the recovery data and produces the recovery clock. The Walsh code demodulator demodulates 16-bit Walsh codes to 5-bit original data after Hamming distance calculation. In the LFSR checker, the same random data sequence as TX is generated by the LFSR circuit. Thus, the LFSR checker can determine whether there have bit errors in random data mode. If the image mode is set, the RX_DATA will be stored in the block memory. Subsequently, the data are transmitted through the UART interface to the PC #2.

The Walsh code modulation in the BCC transceiver increases data reliability, but it also reduces the data rate (or code rate). In standard 16-bit Walsh code [5], to avoid too long CID, the selected code words match the rule that the maximum CID is equal to two, and then the code rate is 1/8. Therefore, the concatenated methods of Walsh codes are proposed to solve the problem of increasing data reliability with relatively high code rate. The chosen code words from 4-bit Walsh codes are concatenated by four 4-bit Walsh codes to form the 16-bit modulated codes. The Hamming distance between each code word ranges from 2 to 8, but the code rate is improved as 5/16. As compared to the standard 16-bit Walsh codes [5] with code rate 1/8, the data rate of the proposed BCC transceiver with concatenated Walsh codes can have 2.5 times speed up.

III. Experimental Results

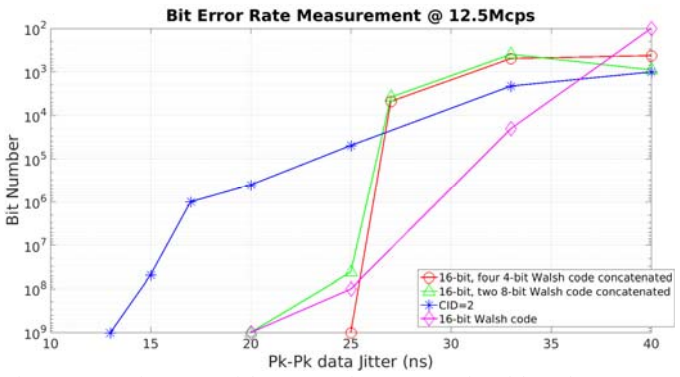

Fig. 2 BER performance of the proposed concatenated Walsh Codes

Fig. 2 shows the first-bit error simulation of the proposed BCC transceiver with data jitter to model the random noise in human body channel communication. The line "CID=2" means the performance of the BCC transceiver without using Walsh codes. The line "16-bit Walsh-code" means the performance of the BCC transceiver with 16-bit standard Walsh codes [5]. At 25 ns peak-to-peak data jitter, the BCC transceiver with 16-bit standard Walsh codes [5] can achieve BER < 10^{-8}. However, the BCC transceiver with CID=2 can only achieve BER < 10^{-5}

The line "16-bit, four 4-bit Walsh code concatenated" means the proposed concatenated method, the BER performance of the four 4-bit Walsh code concatenated method is better than 16-bit standard Walsh codes when peak-to-peak data jitter less than 25 ns. The simulation result shows that the four 4-bit Walsh code concatenated method has better data reliability than the others even this method has smaller Hamming distance between code words.

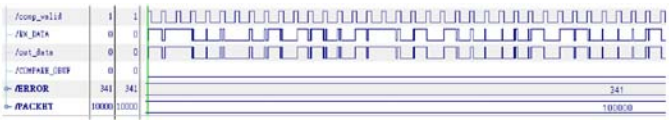

Fig. 3 (a) Measuring bit errors with Xilinx ChipScope Pro analyzer

Fig. 3 shows the measuring bit errors of the proposed FPGA-based BCC transceiver at 12.5 Mcps with Xilinx ChipScope Pro analyzer, and the BER is < 10^{-5}. When the chip rate is less than 6.25 Mcps, there is no bit error after transmission 10^8 bits.

IV. Conclusion

In this paper, an FPGA-based BCC transceiver with concatenated Walsh code method is presented. The measured maximum transmission distance is 140 cm. The maximum chip rate of the proposed BCC transceiver is 12.5 Mcps. With high data reliability, the proposed BCC transceiver can use to transmit an image or a clip of video.

References

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