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A High-Resolution and One-Cycle Conversion Time-to-Digital Converter Architecture for PET Image Applications

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***Abstract*— In this paper, a high-resolution and one-cycle conversion time-to-digital converter (TDC) architecture with cell-based design for positron emission tomography (PET) applications is presented. The proposed TDC employs a cascade-stage structure to achieve high timing resolution and wide sampling range at the same time. Besides, based on the proposed two-level conversion structure, the proposed TDC not only can achieve single cycle latency and high speed of operation, but also have low circuit complexity as compared with conventional approaches. Simulation results show that operation frequency of the proposed TDC can be improved to 200MHz with 50ps resolution. In addition, the proposed TDC can be implemented with standard cells, making it easily portable to different processes and very suitable for biomedical chip applications.**

I. Introduction

Nowadays, positron emission tomography (PET) plays an important role in the cancer diagnosis. PET is a noninvasive diagnosis that measures the in vivo distribution of imaging agents labeled with positron-emitting radioisotopes [1]–[5]. In the beginning of diagnosis, the patient needs to be injected intravenously a positron emitting radionuclide. After positron injects into the body, a positron and an electron annihilate and produce two time-coincident opposing 511-keV gamma rays with 180 degrees apart when two particles contact each other. If the time of flight (TOF) difference between the two opposing gamma ray photons that generated from the annihilation of a positron and an electron can be measured, it can generate a full tomography data set for PET image. In order to measure the timing difference, two gamma ray detectors are placed on opposite sides encircling the body, as shown in Fig. 1 [6].

Fig. 2 illustrates the typical architecture of a PET scanner [7]. The gamma ray detectors detect two opposing gamma rays that hit two detector pairs, and then, the analog front-end circuits generate the event signal. If the incoming gamma-ray event pulse above the threshold, the analog front-end produces a trigger signal. After the time-to-digital converters (TDCs) receive the event signal, the time interval of event signal will be converted into digital codes. The time interval measurement of TDC is shown in Fig. 3. The time difference between the rising edge of START and STOP is required to convert to the digital code. Based on the converted digital codes and digital processing techniques, the PET image can be reconstructed. In the PET image, the signal-to-noise ratio (SNR) is mainly determined by the intrinsic resolution of the detector and the timing resolution of the TDC [5]. In order to improve the quality of PET image, the time resolution of TDC should be smaller than the required coincidence timing resolution of PET image system. Recently, the timing resolution of detector can achieve to 100 ps by the novel scintillator materials [8] and semiconductor-based scintillators [9]. Thus, the timing resolution of TDC should be smaller than 100ps to enhance the image quality.

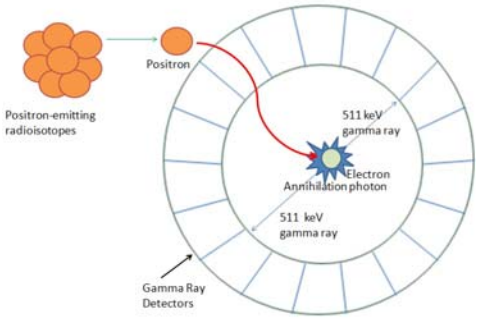

Fig. 1. Annihilation and coincidence detection.

In addition to the timing resolution, the conversion time is another important design consideration in TDC for PET image system application [9]. In terms of the healthcare costs, the short detection response time can reduce the usage time of imaging equipment per patient. As a result, how to improve the conversation rate of TDC is also an important design consideration for PET image application. Besides, because it requires a large number of pulse-processing front-end electronics to construct a PET scanner, the front-end electronics should be implemented by the low-cost, high-performance, high-stability, and high-integration technology, such as complementary metal oxide semiconductor (CMOS) technology, to improve overall performance and reduce manufacturing cost. As the CMOS technology improves rapidly, the application-specific integrated circuits (ASIC) including a high-performance TDC for PET tomography front-end applications have been proposed [5], [6], [9]-[11] . Implementation of these custom chip into the scanner front-end electronics results in over a 70% cost savings [10].

In this paper, a high-resolution and one-cycle conversion cycle TDC architecture is proposed for PET image applications. The proposed TDC employs a cascade-stage

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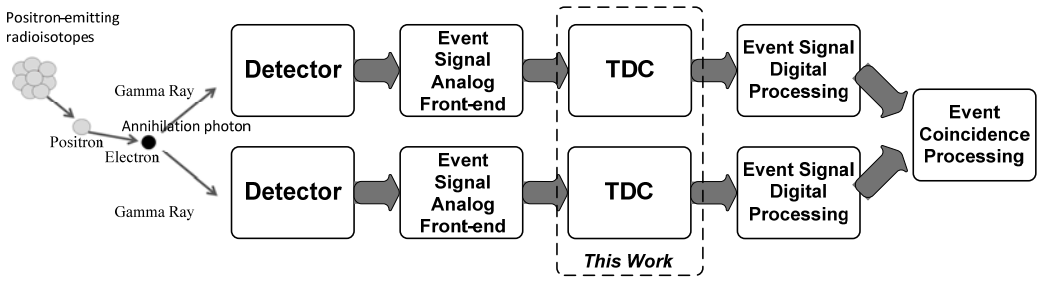

Fig. 2. Block diagram of PET scanner.

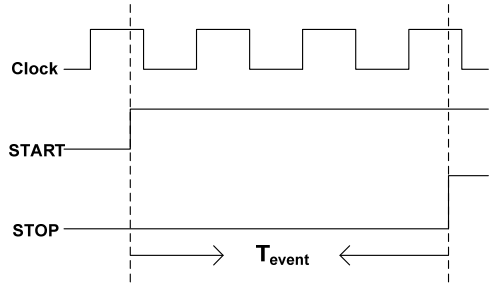

Fig. 3. Time interval measurement in PET scanner.

structure to achieve high timing resolution and wide sampling range at the same time. Besides, based on the proposed two-level conversion structure, the proposed TDC not only can achieve single cycle latency and high speed of operation, but also have low circuit complexity as compared with conventional approaches. In addition, the proposed TDC architecture not only can be implemented by all-digital CMOS design manner for cost and power reduction, but also can be described by hardware description language (HDL) and implemented with standard cells, making it easily portable to different processes and very suitable for biomedical chip applications and system integration.

II. Time-to-Digital Converter Overview

Time-to-digital converters have been widely used for measurement system, temperature sensor, and communication system [12]-[15]. Because TDC can convert the time information to digital code, it is an essential component for the interface of analog and digital signals. Many approaches have been proposed to implement a TDC [12]-[15]. The counter-based TDC uses a high-frequency clock or multi-phase clock to sample the timing interval and convert to multiples of period of high-frequency sampling clock as shown in Fig. 4(a) [12]. The design concept of counter-based TDC is very straightforward, but the quantization time resolution is limited by the counter clock frequency. Another approach is the flash TDC that is analogous to flash analog-to-digital converters (ADCs) for voltage amplitude encoding and operate by comparing a signal edge to various reference edges all displaced in time [13], [14]. The elements that compare the input signal to the reference are usually flip-flops. In the single delay chain flash TDC shown in Fig. 4 (b), each buffer produces a delay equal to τ. It supposes to determine the period of input clock using the eight buffers converter in Fig. 4 (c). Each flip-flop compares the

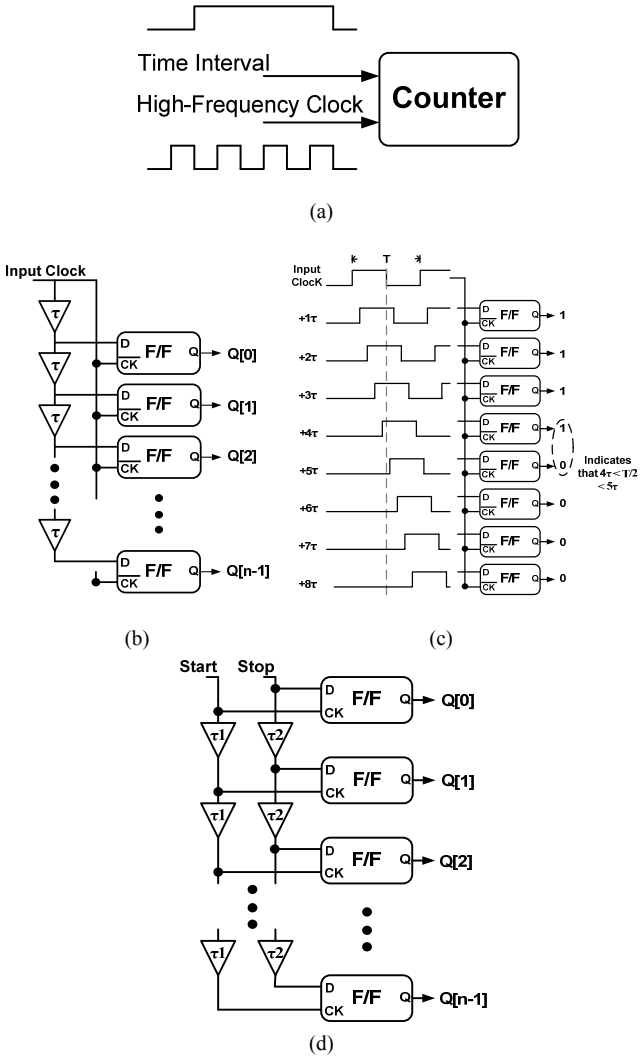

Fig. 4. Different TDC types (a) Counter-based TDC (b) Flash TDC (c) Timing diagram of flash TDC (d) Vernier delay line TDC.

displacement in time of the delayed the first rising edge to the first falling edge of input clock. The thermometer-encoded output indicates the value of delay time of buffer; assuming the flip-flops are given sufficient time to resolve. The drawback to this implementation is that the resolution can not be smaller than a single gate delay, and take long conversion time. In addition, when the frequency of the input clock is low, it will require numbers of flip-flops and buffers to cover large

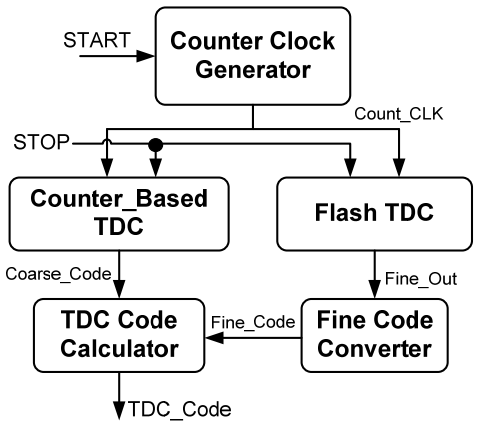

Fig. 5. Block diagram of the proposed TDC.

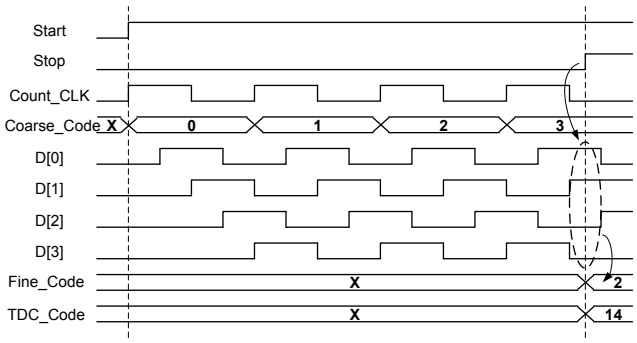

Fig. 6. Timing diagram of the proposed TDC.

clock period, leading to suffer large power consumption and hardware cost. In order to enhance resolution, the flash converter can be constructed with a Vernier delay line as shown in Fig. 4 (d) [15]. This architecture achieves a resolution of t1 - t2, where t1 > t2. However, the power, area, and conversion time issues still need to be resolved when the sampled clock with low frequency. Thus, it needs to propose a novel TDC architecture which can achieve high resolution and high conversion rate at the same time to meet the requirements of PET image system.

III. Proposed Time-to-Digital Architecture

Fig. 5 illustrates the architecture of the proposed TDC, which consists of a counter clock generator, a counter_based TDC, a flash TDC, a fine code converter, and a TDC code calculator. The proposed DCO employs the cascading structure to achieve fine delay resolution and wide sampling range at the same time. Based on the proposed cascading architecture, the proposed TDC can achieve two-level conversion, which can have single cycle latency and low circuit complexity. In the beginning of conversion, the counter clock generator outputs the clock signal for the counter_based TDC when the rising edge of signal START arrives. After the counter_based TDC receives the clock signal, it starts to sample the timing interval and convert to multiples of period of counter sampling clock until the rising edge of signal STOP arrives. The counter clock also sends to the flash TDC, and signal STOP samples the delay cell outputs in flash TDC at the

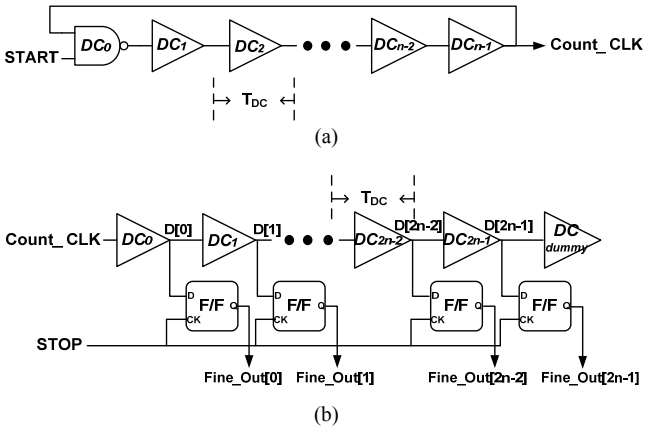

Fig. 7. Circuit implementation (a) Counter clock generator (b) Flash TDC.

rising edge. Consequently, when the rising edge of signal STOP arrives, the flash TDC sampling results (Fine_Out) is converted to Fine_Code, and the TDC code calculator generates the completed TDC code based on the counter_based TDC outputs (Coarse_Code) and Fine_Code. Because the counter_based TDC can convert quickly, it can improve the overall TDC conversion time to one cycle. In addition, the flash TDC can enhance the overall TDC resolution by small delay cell. As a result, the proposed two-level TDC architecture can achieve high resolution and only take one cycle conversion time.

Fig. 6 illustrates the timing waveform of the proposed TDC. In order to simplify the description of TDC operation, the delay time of delay cell in flash TDC is one-fourth of the period of counter clock. Fig. 7(a) and (b) shows the circuit of counter clock generator and flash TDC, respectively. The delay cells in counter clock generator and flash TDC are same. Because the total delay of delay cells in flash TDC is equal to the period of counter clock, the number of delay cell in flash TDC should be double of delay cell in counter clock generator. The TDC output code can be formulated as

$$TDC\_Code = 2 \times N \times X + Y \quad (1)$$

where N is number of delay cell in counter clock generator, X is Coarse_Code, and Y is Fine_Code. The calculation is very sample, implying the hardware cost can be further reduced. In the example of Fig. 6, $N = 2$, $X = 3$, $Y = 2$, and $TDC\_Code = 14$.

IV. Experimental Results

The proposed TDC is designed and implemented by 90nm 1P9M CMOS standard cell library and cell-based design flow, thus the proposed architecture is modeled in Hardware Description Language (HDL) and functionally verified using NC-Verilog simulator, as shown in Fig. 8. Based on the requested frequency range and resolution for PET image application, the design parameters (N) of the proposed TDC are determined to 50. Moreover, we also use transistor-level simulator with Hspice to verify the performance of the timing critical circuits including delay cell and flash TDC. According to the simulation results, the delay of delay cell is 50ps. Thus, the frequency of counter clock is 200MHz. Fig. 8 shows that when the rising edge of STOP arrives, the TDC code

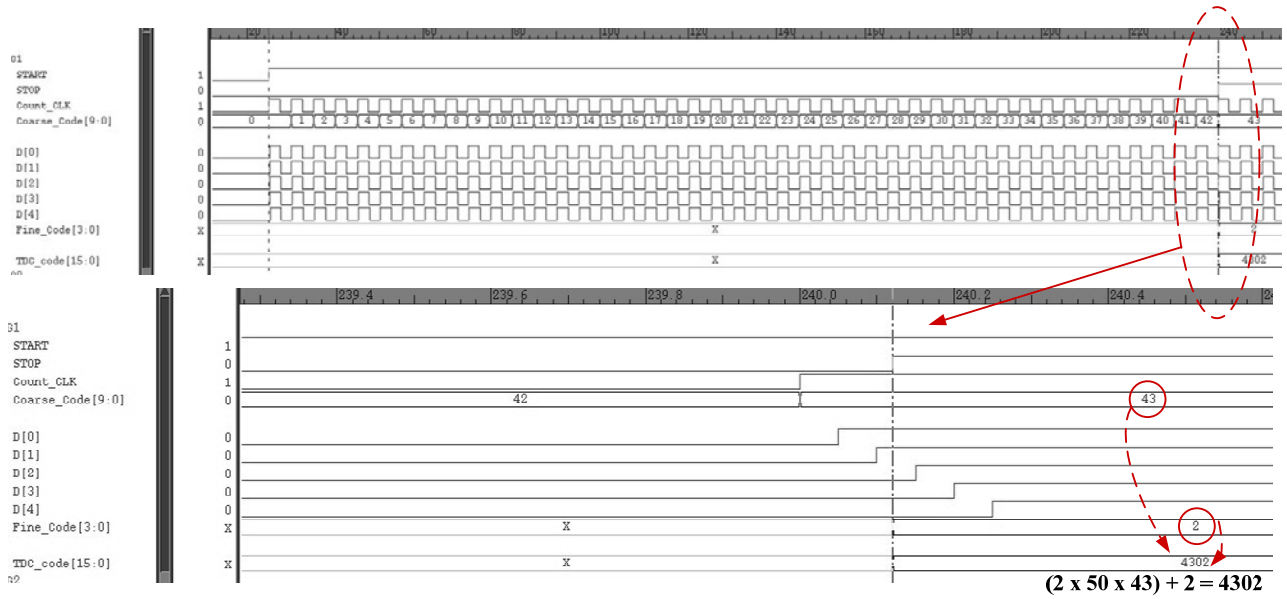

Fig. 8. Simulation results of the proposed TDC.

calculator starts to calculate TDC output code immediately and only takes one event cycle to complete the conversion while keeping high resolution with 50ps.

V. Conclusion

In this paper, we have proposed a high-resolution and high-conversion rate TDC with cell-based design for PET image applications. The proposed TDC employs a cascade-stage structure to achieve high timing resolution and wide sampling range at the same time. The coarse and fine conversion is done by a counter_based TDC and a flash TDC, respectively. Besides, based on the proposed two-level conversion structure, the proposed TDC not only can achieve single cycle latency, but also have low circuit complexity as compared with conventional approaches. Simulation results show that operation frequency of the proposed TDC can be improved to 200MHz with 50ps resolution. Moreover, because the proposed DCO has a good portability as a soft intellectual property (IP), it can reduce both design time and complexity. As a result, it is very suitable for System-on-Chip (SoC) applications as well as system-level integration.

Acknowledgment

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