An All-Digital Clock and Data Recovery Circuit for Spread Spectrum Clocking Applications in 65nm CMOS Technology

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Abstract
In this paper, an all-digital clock and data recovery (ADCDR) circuit is presented. The proposed ADCDR can recover the data stream sent by a transmitter with a spread spectrum clock generator (SSCG). The proposed adaptive gain control scheme can automatically adjust the phase tracking gain by counting the consecutive identical digits (CID), and the time-to-digital converter (TDC)-based fast phase compensation can quickly compensate for a large phase error. The proposed ADCDR can tolerate input peak-to-peak jitter up to 130ps at 480MHz with the down-spread 10% modulation. In addition, the bit error rate (BER) is less than 10^{-12} with 2^{31}-1 pseudo-random binary sequence (PRBS). The proposed ADCDR is implemented in a standard performance 65nm CMOS process with standard cells. The active area is 130μm × 100μm, and the power consumption is 1.13mW at 480MHz with the down-spread 10% modulation.

Keywords
Clock and data recovery (CDR), spread spectrum clock generation (SSCG), phase-locked loop (PLL).

1. Introduction
Nowadays, in many high-speed serial link applications, such as USB 3.0, SATA 3.0, PCI-E 3.0, and DisplayPort, the spread spectrum clock generator (SSCG) is adopted in the transmitter part to effectively reduce the electromagnetic interference (EMI) with low hardware cost. The spreading ratio in a SSCG determines the amount of the EMI reduction, and it also influences the jitter performance of the output clock. In addition, the transmitter with a SSCG produces additional jitter to the receiver, and the bit error rate (BER) of the receiver is increased accordingly. Fig. 1 shows the center-spread spread spectrum clock generation with a triangular modulation profile. The spreading ratio is α, the baseline frequency is F_{center}, and the modulation frequency is f_m in Fig. 1. The average frequency (baseline frequency) in the center-spread modulation should be equal to the non-spread clock frequency, and the spreading ratio determines the maximum and minimum output frequencies of the SSCG. For example, if F_{center} is 160MHz, and the spreading ratio (α) is 10%, the output clock frequency ranges from 152MHz to 168 MHz.

In SATA specifications, the spreading ratio is 5000ppm (0.5%) with a 30 ~ 33 kHz modulation frequency. Thus, the conventional clock and data recovery (CDR) circuit can tolerate the small frequency error produced by the SSCG and still recovers the data correctly. However, if the transmitter can transmit data stream with a larger spreading ratio (>10%), there will be more EMI reduction, as discussed in [1]-[3]. Nevertheless, the frequency error produced by the SSCG will be a design challenge for the CDR circuit design. Therefore, in [4], an adaptive loop filter with a frequency differentiator is proposed to detect the frequency variations during data transmission. However, the CDR circuit [4] requires a non-spread clock as a reference frequency, and thus the frequency error between the transmitter's and receiver's frequency synthesizer should be very small to make this circuit operating correctly. In [5], the dual loop CDR circuit is composed of an analog phase-locked loop (PLL) and a digital CDR. The analog PLL with an external oscillator generates high speed multi-phase clock signals for the digital CDR circuit to recover the data stream with up to ±5000ppm (±0.5%) spreading ratio. However, the CDR circuit [5] requires an external reference clock, and thus the cost and power consumption is increased. In addition, the oversampling architecture usually has higher hardware complexity. As a result, a referenceless and non-oversampling type CDR circuit is preferred for spread spectrum clocking applications with a large spreading ratio (>10%).

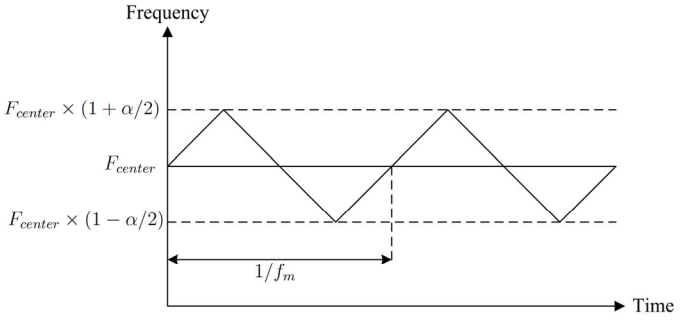

Figure 1: Spread spectrum clock generation.

In this paper, a referenceless all-digital clock and data recovery (ADCDR) circuit with an adaptive gain control scheme and time-to-digital converter (TDC)-based fast phase compensation for spread spectrum clocking applications is presented. The proposed ADCDR circuit adjusts the phase tracking gain by counting the consecutive identical digits (CIDs). In addition, the proposed ADCDR

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can compensate for a large phase error by the proposed TDC. As a result, the frequency variations during data transmission can be easily tracked and compensated for even with a large spreading ratio in the transmitter.

This paper is organized as follows: Section 2 describes the proposed ADCDR architecture. The circuit implementation is discussed in Section 3. Section 4 shows experimental results. Finally, Section 5 concludes with a summary.

2. Architecture Overview

Fig. 2 shows the proposed referenceless all-digital CDR (ADCDR) architecture. It is composed of a dual-mode phase and frequency detector (PFD) [6], a time-to-digital converter (TDC), a digital loop filter (DLF) [7], an ADCDR controller, and a monotonic low-power digital controlled oscillator (DCO) [8]. After system is reset, the input data is delayed and exclusive-OR with the original input data to generate the data transition signal (Data_T). The dual-mode bang-bang PFD [6] is applied to detect the frequency and phase error between Data_T and DCO clock (DCO_Clk) to the ADCDR controller with random data patterns input. The phase error information is quantized by the TDC for the accumulated phase error compensation. The DLF [7] receives the dco_code[9:0] and produces the baseline DCO control code to filter out the input data jitter effects. The DCO [8] is applied in the proposed ADCDR circuit, and it has a monotonic response between the DCO control code and the output frequency. In addition, the proposed DCO is composed of a ladder-shaped coarse-tuning stage and an interpolating fine-tuning stage for wide frequency range operation with a high resolution and low-power consumption.

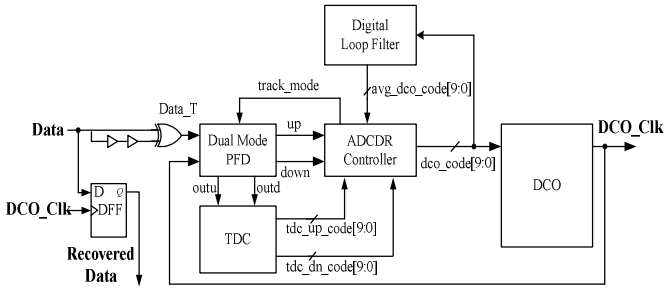


Figure 2: The proposed ADCDR.

The proposed ADCDR controller performs three functions. First, the modified binary search algorithm [9] is applied for the fast frequency and phase acquisition in the beginning. Second, the adaptive gain control with CID (AGCID) scheme is proposed to automatically adjust the phase tracking gain. Third, the TDC-based fast phase compensation is proposed to compensate for a large phase error and maintain the frequency and phase stability. In conventional bang-bang CDR architecture, the phase tracking ability is very poor, and it is because only the bang-bang phase information is used to control the DCO. However, there is no data transition in the CID region, and the frequency error is accumulated in this region and may cause a large phase error in the end of the CID region. Thus, the proposed AGCID scheme and the TDC-based fast phase compensation approach can enhance the proposed ADCDR's phase and frequency tracking ability. Hence, the frequency variations during data transmission can be easily tracked and compensated for even with a large spreading ratio in the transmitter.

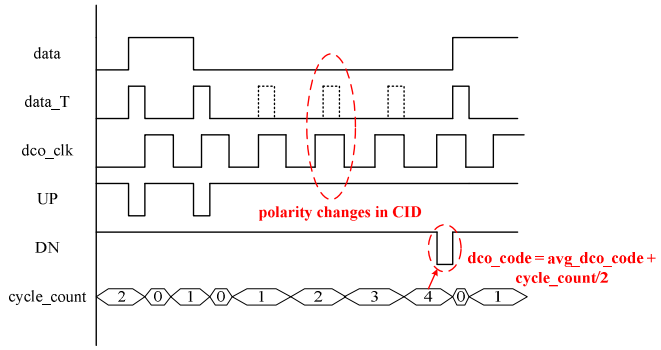


Figure 3: Polarity changes in the CID region.

After frequency and phase acquisition is completed, the CID length (cycle_count) is counted, as shown in Fig. 3. The cycle_count is cleared whenever the data transition occurs. If there is no phase polarity change in the end of the CID region, it means that there are consecutive up or down pulses in the CID region. Thus, the proposed AGCID scheme will add or subtract the DCO control code by the CID length (cycle_count). As a result, the accumulated phase error is quickly compensated in the end of each CID region. Oppositely, if there are phase polarity changes in the end of the CID region, it means the phase polarity is changed during the CID region. However, we cannot identify where the polarity change occurred in the CID region, so we assume the phase polarity is changed in the middle of the CID region. As a result, the proposed AGCID scheme will restore the baseline DCO code (avg_dco_code) calculated by the DLF, and then adds or subtracts the DCO control code by the CID length (cycle_count) divided by 2.

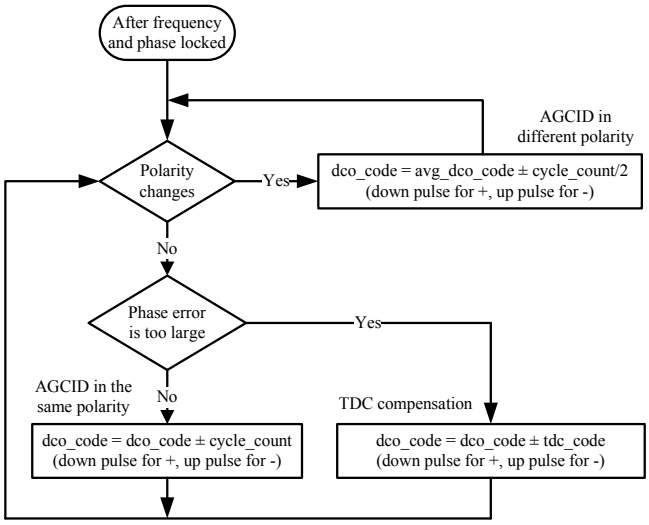


Figure 4: The proposed AGCID and TDC compensation flow.

Fig. 4 shows the flow chart of the proposed AGCID scheme and the TDC-based fast phase compensation. If the ADCDR controller detects consecutive up or down pulses,

and the accumulated phase error is smaller than 1/3 clock period. Then, the DCO control code will be added or subtracted by the CID length (cycle_count) according to the PFD's output. In this case, if the accumulated phase error is too large (> 1/3 clock period), the phase error is compensated for by a larger phase tracking gain (tdc_code) to quickly reduce the phase error. Oppositely, if the ADCDR controller detects phase polarity is changed in the end of the CID region, the baseline DCO control code (avg_dco_code) is restored to the DCO control code (dco_code) with an offset (cycle_count/2). When the phase polarity is changed during the CID region, the accumulated phase error will be a small value, and thus the TDC code (tdc_code) is not used in this situation.

3. Circuit Implementation

Fig. 5 shows the proposed TDC circuit. A digital pulse amplifier is applied in the TDC to extend the input signal's pulse width. Thus, the signal (Pulse_amp) can be used to reset the TDC delay line after each TDC operation. The PFD outputs a low pulse to the TDC, and the input signal passes through the TDC delay line which is composed of the TDC delay units (TDUs). The output of each TDU is sampled at the positive edge of the input signal. Thus, the input pulse width (i.e. phase error) can be quantized by the delay time of the TDU. In the proposed TDC circuit, the TDC resolution is about 84ps.

The monotonic low-power DCO architecture [8] is applied in the ADCDR circuit design. The DCO ranges from 119MHz to 550MHz with a 102ps coarse-tuning resolution and a 6.4ps fine-tuning resolution. The power consumption of the proposed DCO is 483µW at 550MHz. In addition, the dual-mode PFD [6] is applied in the proposed ADCDR circuit design, and the proposed PFD has a dead zone about 3ps.

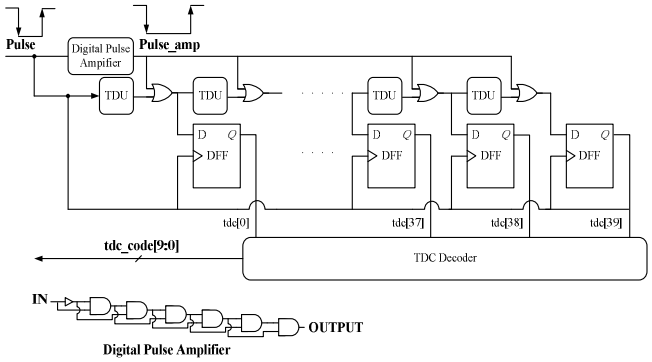


Figure 5: The proposed TDC circuit.

4. Experimental Results

The proposed ADCDR is implemented in a standard performance (SP) 65nm CMOS process with standard cells and a 1.0V power supply. Fig. 6 shows the layout of the proposed ADCDR circuit. The active area is 130µm × 100µm. The frequency range of the proposed ADCDR ranges from 160MHz to 480MHz, and the power consumption is 1.13mW at 480MHz with the down-spread 10% modulation.

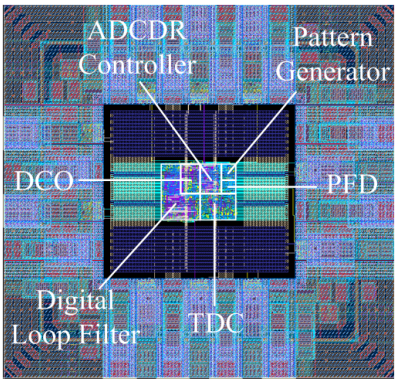


Figure 6: Layout of the proposed ADCDR.

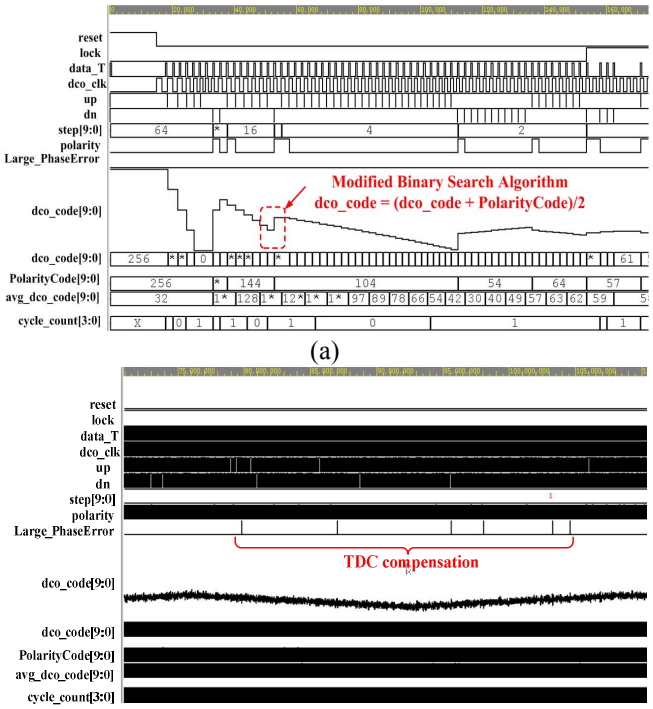


Figure 7: Simulation Results (a) Modified binary search algorithm (b) Random data tracking with SSC.

A pattern generator is included in the test chip. It can perform the down-spread 10% modulation with a 30 kHz modulation frequency. Fig. 7 shows the simulation result of the proposed ADCDR. In the beginning, the ADCDR controller performs modified binary search algorithm [9] to achieve frequency and phase acquisition in a short time, as shown in Fig. 7(a). In Fig. 7 (a), the PolarityCode is the previous recorded DCO control code at phase polarity change. When the phase polarity is changed again, the DCO control code is updated as the average value of dco_code and PolarityCode. As compared to the binary search algorithm with a digital loop filter [7], the modified binary search algorithm [9] can quickly find the DCO control code close to the target DCO control code in a short time. Then, the ADCDR controller returns to its normal opeation, as discussed in Fig. 4.

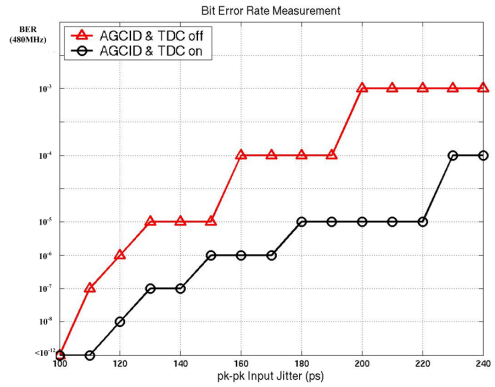
Fig. 7 (b) shows the frequency and phase tracking with random data patterns and the spread spectrum clock (SSC).

The input data stream has a down-spread 10% modulation at 480MHz. The proposed AGCID scheme and the TDC-based fast phase compensation approach are applied to track the frequency variations due to the down-spread modulation during data transmission. The Large_PhaseError signal indicates that the phase error is too large (> 1/3 clock period) in these cycles, and the phase error is compensated for by a larger phase tracking gain (tdc_code) to quickly reduce the phase error. Finally, in Fig. 7(b), the DCO control code over time has a down-spread triangular profile, since the proposed ADCDR keeps tracking the frequency variations of the received data stream.

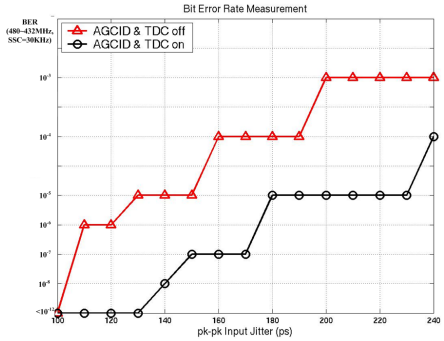
Fig. 8 shows the BER performance of the proposed ADCDR. When the data is transmitted without the down-spread spread spectrum modulation, the proposed AGCID scheme and the TDC-based fast phase compensation approach can improve the jitter tolerance of the CDR circuit. In Fig. 8(b), when the data is transmitted with the down-spread 10% modulation and the SSCG in the transmitter outputs frequency ranges from 432MHz to 480MHz. The proposed AGCID scheme and the TDC-based fast phase compensation approach can enhance the phase and frequency tracking ability. Therefore, the jitter tolerance is improved to 130ps as compared to without the ADCID and the TDC. As a result, the frequency variations during data transmission can be tracked and compensated for even with a 10% spreading ratio in the transmitter.

5. Conclusion

In this paper, a referenceless all-digital clock and data recovery circuit with the adaptive gain control scheme and the TDC-based fast phase compensation approach is presented. With the AGCID and TDC-based fast phase compensation, the jitter tolerance can be increased from 100ps to 130ps with 432MHz to 480MHz spread spectrum clock. Besides, the proposed ADCDR circuit is implemented with standard cells, and thus it has good portability over different processes. As compared with existing solutions, the proposed ADCDR can recover the data stream with a large spreading ratio. Thus, the proposed ADCDR is very suitable for high speed serial link application in SoC era.



(a)



(b)

Figure 8: BER performance (a) 480MHz Non-SSC (b) 432MHz to 480MHz SSC.

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