An All Digital Spread Spectrum Clock Generator with Programmable Spread Ratio for SoC Applications

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***Abstract*—In this paper, a programmable all-digital spread spectrum clock generator (ADSSCG) suitable for System-On-Chip (SoC) applications with ultra-low-power capability is presented. Based on the timing constraint of system, the programmable ADSSCG can provide the suitable frequency spread ratio to obtain the optimal combination of timing deviation and EMI reduction for system applications. Besides, the proposed ADSSCG employs an ultra-low-power digitally controlled oscillator (DCO) to save overall power consumption to 560μW (@400MHz) and the peak EMI power reduction is large than 25dB. In addition, the proposed ADSSCG can be implemented only with standard cells; as a result, the area can be saved without any passive component, and making it easily portable to different processes and very suitable for SoC applications.**

I. INTRODUCTION

As the operating frequency of electronic systems increases, the electromagnetic interference (EMI) effect becomes a serious problem in modern IC designs. Thus, the radiated emissions of system should be kept an acceptable level to ensure the function and performance of system and adjacent devices [1]. Many approaches have been proposed to reduce EMI, such as shielding box, skew-rate control, and spread-spectrum clock generator (SSCG). Because SSCG modulates the system clock directly which is the major contributor of system EMI, it can lower the radiated emission significantly with less increase of extra cost [1], [2] and becomes the most popular solution among these techniques for SoC applications.

Recently, different architectural solutions have been developed to implement SSCG. The most straightforward method is to modulate the control voltage of a voltage-controlled oscillator (VCO) in a phase-locked loop (PLL) [1]-[3]. Although this method can provide good performance in EMI reduction, it requires large loop filter component to pass modulated signal in a PLL, resulting in chip area increasing or off-chip capacitor requirement and power increasing [2], [3]. Modulation on divider is another important SSCG type that utilizes a fractional-N PLL with delta-sigma modulator to spread output frequency by divider ratio changing in PLL [4]-[7]. Traditionally, these conventional SSCGs are designed by analog approach, however, as supply voltage decreases, both gain and frequency range need to be traded off in VCO which is the most important component in SSCG. Thus, it has to take more design efforts to integrate analog SSCGs in SoC with lower supply voltage and advanced process. Furthermore, as technology migrates, the analog blocks in SSCG need to be re-designed. In contrast to analog type SSCG, all-digital SSCG [8] that does not utilize any passive components and use digital design approach has been proposed. Although [8] use digital design approach, the fully custom design is still required for the delay line, resulting in long design cycle and low portability. Besides, it needs an extra PLL to provide spread-spectrum clock signal for system operation.

In this paper, a portable SSCG with the triangular modulation and an ultra-low-power digitally controlled oscillator (DCO) is proposed for SoC applications. The proposed ADSSCG employs the novel triangular modulation to provide wide programmable spread-ratio, low circuit complexity, and high EMI attenuation. In addition, the proposed ADSSCG, including the DCO, can be described by HDL language and implemented with standard cells, making it easily portable to different processes and very suitable for SoC applications.

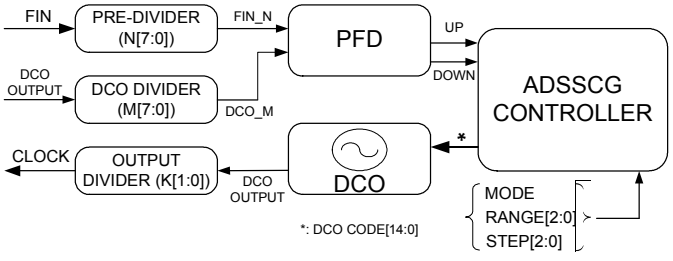

Figure 1. The proposed ADSSCG architecture

II. ARCHITECTURE OVERVIEW

Fig. 1 is the proposed ADSSCG architecture. There are several functional blocks: phase/frequency detector (PFD), ADSSCG controller, DCO, and three frequency dividers (pre-divider, DCO divider, and output divider). Through the DCO divider and output divider, the signal DCO_M and the system required clock signal CLOCK is the output of DCO divided by M and K respectively, and FIN_N comes from input reference clock divided by N. The ADSSCG can provide the clock signal with or without spread-spectrum function based on the operation mode setting. In the normal operation mode, ADSSCG operates as an ADPLL to generate a fixed frequency clock output. The PFD generates the signal "UP" or "DOWN" depending on the phase and frequency difference between FIN_N and DCO_M. If DCO_M leads FIN_N, PFD generates a "DOWN" signal to slow down the DCO. Conversely, when DCO_M lags FIN_N, PFD generates a "UP" signal to speed up the DCO. When the ADSSCG controller receives "UP" or "DOWN" from the PFD, it changes the DCO control code (DCO CODE [14:0]) to control the DCO to generate the output clock (DCO_OUTPUT). These blocks form a close-loop to achieve the "phase-locked" function. In the spread-spectrum operation mode, the ADSSCG controller generates the DCO control code with triangular modulation based on the spread-spectrum control signals (RANGE [2:0] and STEP [2:0]) to modulate the frequency of DCO output clock with specified spread-ratio and reduce the peak EMI power of system clock.

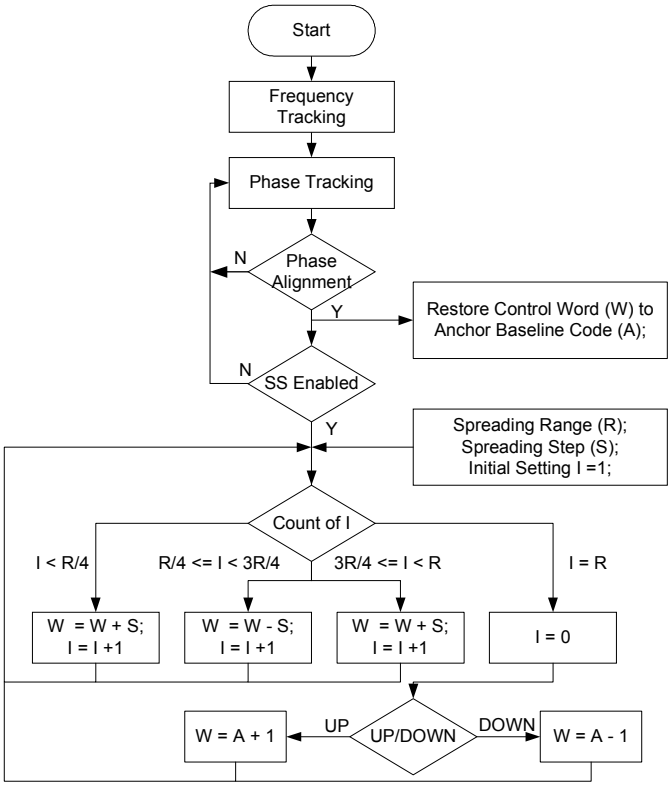

Figure 2. The flowchart of spread-spectrum algorithm

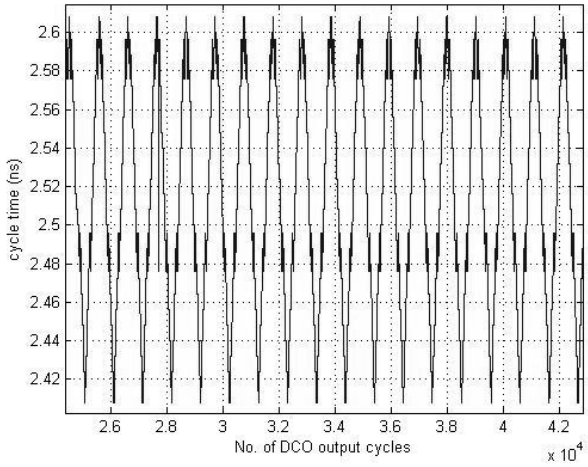

Figure 3. Transient of triangular modulation

III. SPREAD-SPECTRUM ALGORITHM

The proposed ADSSCG has two operation modes: normal operation mode and spread-spectrum operation mode. Fig. 2 shows the flowchart of spread-spectrum operation mode. Before the spread-spectrum operation mode starts, the "locked" DCO control code will be restored into the anchor register to keep the baseline frequency. The triangular modulation means the DCO output frequency is equal to baseline frequency in the beginning, and it will take one-fourth of modulation cycle time to reach the maximum frequency, and then takes half of modulation cycle time to reach the minimum frequency. Finally, it will return to the baseline frequency in the last one-fourth cycle time. Once it completes one modulation cycle, the baseline control code will be updated by PFD output to enhance the phase tracking capability. Two control signals, spreading range (R) and spreading step (S), are specified from the system required to control the triangular modulation. Spreading step is the changing size of DCO control code in each code changes within the triangular modulation. Spreading range determines the period of the triangular cycle that means how many steps are in one triangular cycle. The spread-ratio of frequency equation can be given as

$$SR = (S \times D \times R / 2) / Tc \times 100\% \qquad (1)$$

where SR is the spread-ratio, D is the minimum delay step of DCO, and Tc is the central period of DCO output clock. For example, as shown in Fig.3, if the spreading range is 256, spreading step is 2, the minimum delay step of DCO is 1ps, and the DCO output clock is 400MHz, and then the spread-ratio equals to 10.24%.

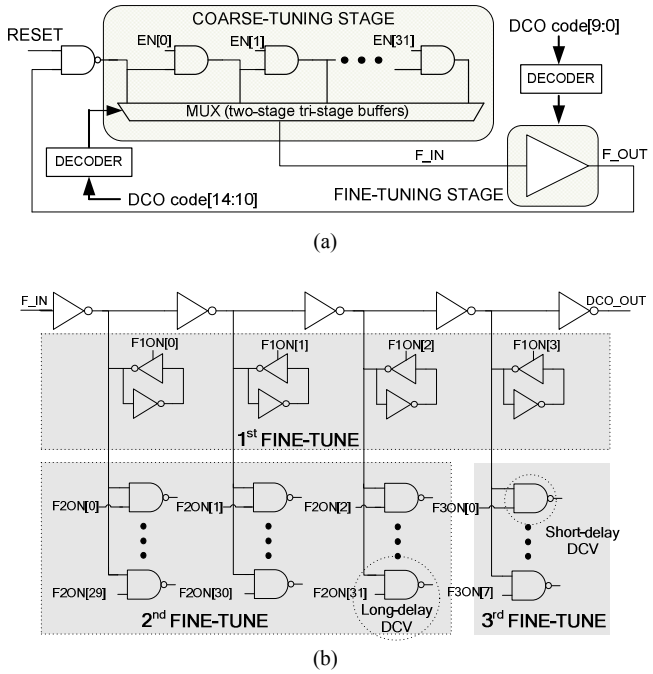

Figure 4. (a) Architecture of the proposed DCO (b) Three fine-tuning stages

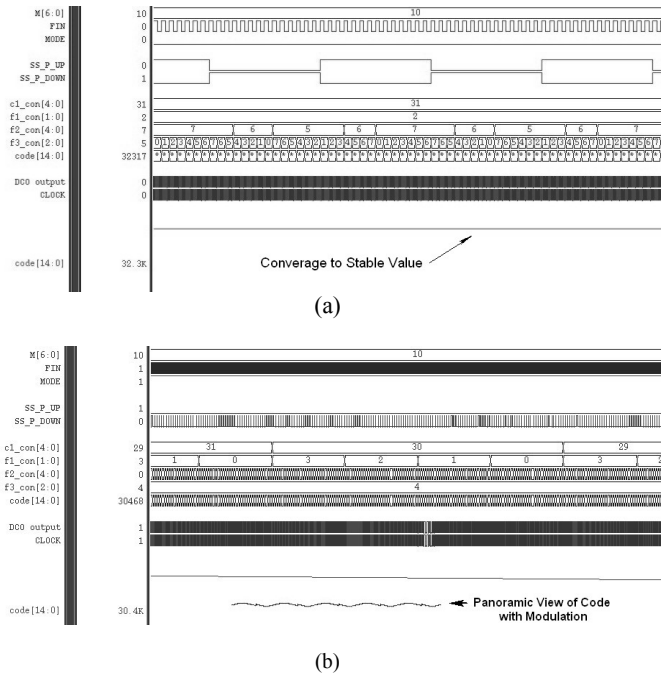

Figure 6. (a)Simulation results of normal operation mode (b) Simulation results of spread-spectrum operation mode

IV. DIGITALLY CONTROLLED OSCILLATOR

The most important circuit design consideration of ADSSCG is how to reach a high-resolution and low-power DCO. Fig. 4(a) illustrates the architecture of the proposed ultra-low-power DCO. To preserve the control code resolution and operation range, the proposed DCO employs cascading structure for both coarse-tuning and fine-tuning stages to maintain control code-to-delay linearity and extend operation range easily. In the coarse-tuning stage, there are 32 different paths and only one path is selected by the 32-to-1 path selector MUX. In order to reduce the loading capacitance of MUX output, we use two-stage tri-stage buffers to form this MUX. In order to reduce power consumption, the coarse-tuning delay cell utilizes a two-input AND gate which can be disabled when the DCO operates at high frequency. In order to increase the frequency resolution of DCO, the three fine-tuning stages are added into the DCO design as shown in Fig.4 (b). The 1st stage is composed of eight 1st fine-tuning delay cells and each of which contains one inverter and one tri-stage inverter. These delay cells are controlled by the control signals (F1ON [0] ~ F1ON [3]). When the tri-stage inverter in 1st fine-tuning delay cell is enabled, the output signal of enabled tri-stage inverter has the hysteresis phenomenon. Thus the delay cell can achieve different delay time [9]. To achieve better resolution capability, different digitally controlled varactors (DCVs) are exploited in the 2nd and 3rd fine-tuning stages to improve the overall resolution of DCO. The operation concept of DCV is to control the gate capacitance of logic gate with input state to adjust the delay time [10]. The 2nd and 3rd fine-tuning stages employ 32 long-delay DCV cells (two-input NAND with strong driving capability) and 8 short-delay DCV cells (two-input NAND with weak driving capability) respectively. From the simulation results, the proposed DCO can achieve 270μW (@400MHz) with 1ps resolution.

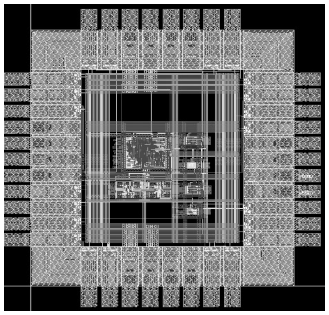

Figure 5. Layout of ADSSCG test chip

V. IMPLEMENTATION AND SIMULATION RESULTS

The proposed ADSSCG is designed by cell-based design flow. We use Hardware Description Language (HDL) to design and describe the test chip of the ADSSCG, which is implemented in 90nm 1P9M CMOS process, where layout of the ADSSCG chip is shown in Fig.5. Fig.6 shows the simulation results of transient response of the ADSSCG in two different operation modes, where the reference clock is 20MHz, and the division ratio (M) is 10, thus the output frequency is 200MHz (=20MHz * 10). In Fig. 6, we can see that the DCO control code will be converged to a stable value in the normal operation mode, and modulated with a spreading value in the spread-spectrum operation mode respectively. Fig. 7 shows the

TABLE I. COMPARISON WITH EXISTING SSCGS

Performance Indices	Proposed	JSSC'03 [2]	IEICE'06 [6]	JSSC'07 [8]
Process	90nm CMOS	0.35μm CMOS	0.35μm CMOS	0.15μm CMOS
Design Approach	All-Digital	Analog	Analog	All-Digital
Modulation Method	Modulation on DCO	Modulation on VCO	Modulation on Divider	Delay Line
Output Frequency (MHz)	191 ~ 952	66/133/266	300	27
Spread Ratios (%)	User-Defined	0.5, 1, 1.5, 2, 2.5	0.4, 0.8, 1.6, 3.2	3
EMI Reduction (dB)	25	NA	20.54 @3.2%	13
Power consumption	560 μW (@400MHz)	300mW (@266MHz)	17.5mW (300MHz)	7.1mW (@27MHz)
Area (mm x mm)	0.24 x 0.3	1.36 x 1.48 (Excluding loop filter)	0.63 x 0.62	0.06
Portability	Yes	No	No	No

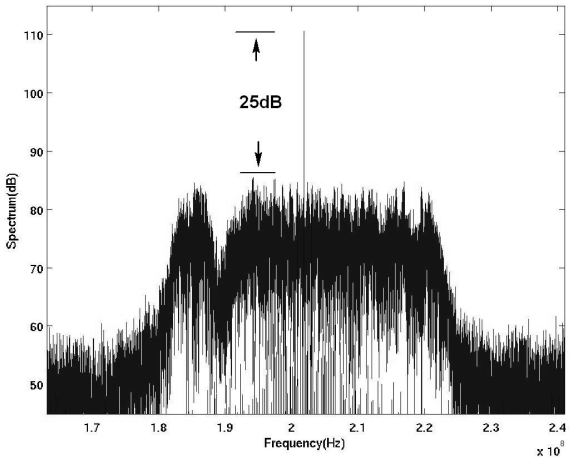

Figure 7. FFT simulation of ADSSCG

FFT simulation results of normal clock signal and spread-spectrum clock signal, and the peak attenuation is 25dB at 200MHz with 20% spread-ratio. Table I lists comparison results with the state-of-the-art SSCGs. The proposed triangular modulation can provide the user-defined spread-ratio and does not induce any performance loss. Additionally, since the proposed SSCG can be implemented with standard cells, it has a good portability. As a result the proposed SSCG has the benefits of better EMI reduction, power consumption, operation range, area, and portability.

VI. CONCLUSIONS

In this paper, a portable ADSSCG with programmable spread-ratio has been proposed. Based on the proposed triangular modulation, the spread-ratio can be specified flexibly by user. The peak attenuation of system clock can be reduced 25dB, and power consumption is 560μW (@400MHz). In addition, the proposed ADSSCG utilize a high-resolution and low-power DCO that consists of one coarse-tuning stage and three different fine-tuning stages. Since all designs of the proposed ADSSCG are described with HDL language, it can be ported to different processes easily, making our proposal very suitable for system-level and SoC applications.

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