

A Fast-Lock-In ADPLL with High-Resolution and Low-Power DCO for SoC Applications

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Abstract—In this paper, we propose a fast-lock-in all-digital phase-locked loop (ADPLL), which is designed with the cell library and described by Hardware Description Language (HDL). The proposed ADPLL uses a novel 2-level flash time-to-digital converter (TDC) to lock in within 2 reference clock cycles. The novel digitally controlled oscillator (DCO) achieves high-resolution with 0.93ps resolution and can extend the controllable range easily. In addition to high-resolution, the power consumption of the proposed DCO can be lowered as 110 μ W(@200MHz). The proposed ADPLL can be easily ported to different process as a soft intellectual property (IP), making it very suitable for System-On-Chip (SoC) applications as well as system-level power management.

I. INTRODUCTION

Phase-locked loop (PLL) is a very important clocking IP for many digital systems such as digital communication and microprocessor. It can be used for frequency synthesis, clock de-skew, and duty-cycle enhancement. Traditionally, the PLL is designed by analog approaches. However, in the SoC era and deep-sub micro technology, integrating an analog block into a digital system needs to take more design efforts. Furthermore, as the technology migrates, the analog blocks need to be re-designed. In contrast, all-digital phase-locked loop (ADPLL) uses the cell-based design approaches, so it can be easily integrated into the digital system. In addition, the ADPLL has the higher immunity for switching noise, and process, voltage and temperature (PVT) variations.

As the chip density increases, the power management scheme becomes more and more important in SoC design. Many systems have the sleep mode to save power consumption. When the system exits the sleep mode to enter normal active mode, the clock generator should provide the system clock as soon as possible [1]. The proposed ADPLL uses the novel 2-level flash TDC to achieve lock-in time within two reference clock cycles. This unique feature is very attractive for low-power system design with fast entry and exit power management techniques.

The digitally controlled oscillator (DCO) is the heart of ADPLL. Just like the voltage-controlled oscillator (VCO) in PLL, DCO provides the ADPLL output clock signal. The most important design consideration of ADPLL is how to

design a high-resolution and low-power DCO. Since the major jitter source of ADPLL comes from the DCO, the high-resolution DCO can reduce the jitter of ADPLL significantly. The proposed novel DCO can achieve 0.93ps resolution and the controllable range can be extended easily, thus the proposed ADPLL can achieve low-jitter operation. In addition to resolution and operation range, power consumption becomes more important in SoC applications. Since DCO occupies over 50% power consumption of ADPLL [2], reducing DCO power consumption is very important for low-power ADPLL design.

This paper presents a new ADPLL solution for SoC applications. The proposed ADPLL can be implemented with cell library. Including the DCO, all designs of ADPLL can be described with HDL language. Because its portability, it can be used as a soft IP, and it is very suitable for SoC design since both design time and complexity can be reduced. Since the proposed DCO can achieve both high resolution and low power, it can meet the demands of system-level integration.

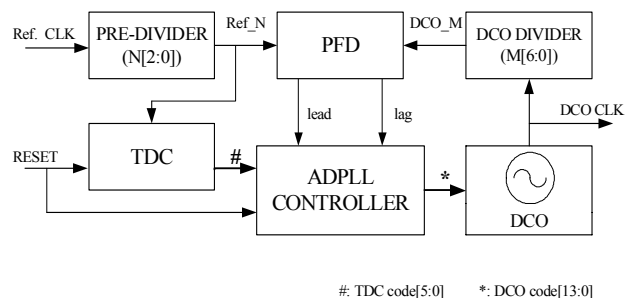


Figure 1. The proposed ADPLL architecture

II. ARCHITECTURE OVERVIEW

Fig. 1 is the proposed ADPLL architecture. There are several functional blocks: TDC, phase/frequency detector (PFD), ADPLL controller, DCO, and two frequency dividers (pre-divider and DCO divider). Through the DCO divider, the signal DCO_M is the output of DCO divided by M. The Ref_N comes from reference clock divided by N. Once the

ADPLL is enabled, TDC provides the coarse DCO control code (TDC_code [5:0]) to the ADPLL controller after two reference clock cycles, and then DCO generates the desired frequency output by this coarse DCO control code. After TDC operation is completed, the PFD generates the signal “lead” or “lag” depending on the phase and frequency difference between Ref_N and DCO_M. If DCO_M leads Ref_N, PFD generates a “lead” signal to slow down the DCO. Conversely, when DCO_M lags Ref_N, PFD generates a “lag” signal to speed up the DCO. When the ADPLL controller receives “lead” or “lag” from the PFD, it changes the DCO control code (DCO_code [13:0]). And then DCO control code controls the DCO to generate the output clock (DCO_CLK). These blocks form a close-loop to achieve the “phase-locked” function.

III. FAST-LOCK-IN MECHANISM

In SoC design, the power management scheme becomes more and more important. Many systems have the sleep mode to save power consumption. To reduce the power consumption in the sleep mode, the clock signal should be turned off. In order to further reduce power consumption, clock generator should be shut down simultaneously. When the system exits the sleep mode to enter normal active mode, the clock generator should provide the system clock as soon as possible [1]. Here, we propose a novel 2-level flash TDC to obtain the desired DCO output frequency within two reference clock cycles. After TDC operation is completed, ADPLL enters the phase tracking mode.

A. A Novel 2-level Flash TDC Architecture

The TDC is used to convert the timing information to the digital codes. During TDC operation, the period of reference clock divided by N (Ref_N) can be quantized as the multiples of delay cell that forms the DCO coarse-tuning stage. After ADPLL controller receives the TDC output code (TDC_code [5:0]), the DCO control codes are determined to generate the desired DCO output clock. There are many approaches to implement a TDC [2]–[4]. The counter-based TDC [2] uses a high-frequency clock or multi-phase clock to sample the timing interval. Utilizing a vernier delay line can enhance TDC resolution [3]. Because every delay cell output in single level flash TDC is sent to one D-flip-flop [4], it need many D-flip-flops, increasing much area and power. In contrast to single level type, our proposed design takes only 12 D-flip-flops (8+4), thus it can reduce hardware complexity and power consumption.

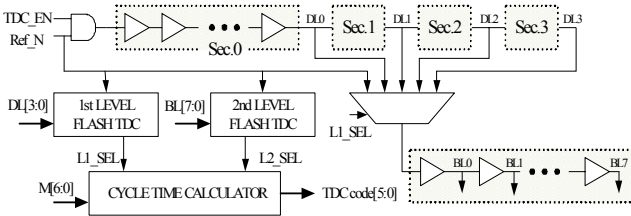


Figure 2. The proposed 2-level flash TDC architecture

Fig. 2 shows the proposed 2-level flash TDC architecture. There are several functional blocks, namely one long delay chain, one short delay chain, 1st level flash TDC, 2nd level flash TDC, path selection multiplexer, and cycle time calculator. The long delay chain consists of 32 delay cells, and these delay cells are partitioned into four sections (Secs.0~3). In contrast to long delay chain, the short delay chain has only 8 delay cells. All delay cells used in long and short delay chain remain the same as those for DCO coarse-tuning stage. When the TDC is enabled, Ref_N is sent to the long delay chain, and all outputs (DL [3:0]) are sent to the 1st level flash TDC. When the first falling edge of Ref_N arrives, the 1st level flash TDC generates the section selection signal (L1_SEL) to select one of section outputs for the short delay chain. Then the 2nd level flash TDC generates the delay selection signal (L2_SEL) based on the delay outputs (BL [7:0]). The section and delay outputs are thermometer code type that can be used to generate selection signals easily. When both L1_SEL and L2_SEL have been generated, the cycle time calculator can estimate the period of Ref_N. The conversion equation can be given as

$$Tr = (L1_SEL \times 8 + L2_SEL) \times 2 \quad (1)$$

where Tr is the period of Ref_N. For example, as shown in Fig. 3, if the period equals to 36 times of delay cell delay time, L1_SEL and L2_SEL should be 2 and 2 respectively. To reduce lock-in time, the TDC only measures half period of Ref_N, thus the calculated value should be shifted left to obtain one Ref_N cycle time.

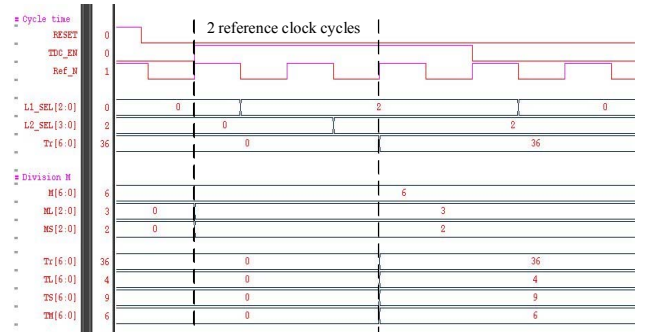


Figure 3. Simulation of the proposed 2-level flash TDC architecture

In the proposed ADPLL architecture, the frequency of Ref_N should be the same as the frequency of DCO divided by M (DCO_M). The delay time of coarse-tuning stage in DCO equals Tr divided by M. In order to reduce the hardware complexity of division, we propose a novel method to approximate this division operation results. This simplified operation can be divided into two steps. First, if the value of division ratio (M) is the power of two, this division operation is only a shift-right operation. If not, we extract the value of power of two of MSB in M (MS) and add one to MS. Second, the division ratio will be shifted

right by MS and ML (MS+1), and then the division results (TM) equals the average of these two values (TL and TS). Simulation results of the novel 2-level flash TDC is shown in Fig. 3. The TDC takes only two reference clock cycles to complete lock-in operation. Because the TDC resolution equals delay time of one delay cell (165ps), the frequency error is 3.3% (@ 200MHz) in the lock-in state.

B. Phase Tracking Mode

After TDC operation is completed, ADPLL takes one reference cycle time to align phase and enter the phase tracking mode. This mode is to track phase of the reference clock depending on the results of PFD outputs. By the pulse amplifiers and the signal expanders, the minimum detectable phase error of the PFD is 5ps [5]. When the PFD output changes from “lead” to “lag” (or vice versa), the search step is reduced by one half of the previous step. If the direction remains the same for eight times, the search step jumps twice as the previous step to accelerate phase tracking.

IV. DIGITALLY CONTROLLED OSCILLATOR

The most important design consideration of ADPLL is how to reach a high-resolution and low-power DCO. In [1] and [6], the DCO consists of many binary-weighted width MOS to achieve high resolution. However, it needs full-custom design and takes longer design time once process changes. Some proposals use tri-state buffers to build the DCO [7]-[8], where different delay path is selected to meet target timing. The proposed DCO can achieve 0.93ps resolution, where power consumption of ADPLL is only 110 μ W(@200MHz).

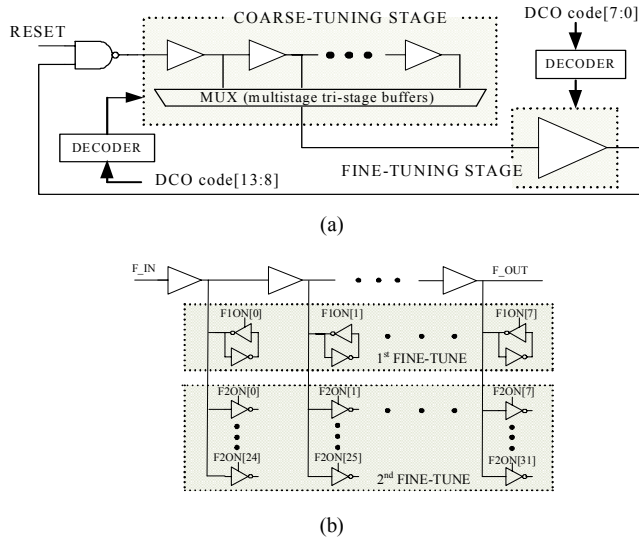


Figure 4. (a) Architecture of the proposed DCO (b) 1st and 2nd fine-tuning stage

A. High-Resolution and Low-Power DCO Architecture

Fig.4 (a) shows architecture of the proposed DCO, which consists of three stages, namely coarse-tuning stage, 1st fine-tuning stage, and 2nd fine-tuning stage. First, in the coarse-tuning stage, there are 64 different paths and only one path is selected by the 64-to-1 path selector MUX. In order to reduce the loading capacitance of MUX output, we use multistage tri-stage buffers to form this MUX [5], [7]. The supply voltage for DCO can be lowered to reduce power consumption of DCO. Since the supply voltage is lower, it needs fewer delay cells to obtain the same delay time and hence area and power can be saved. In order to further reduce power consumption of DCO, the 64 coarse-tuning delay cells are divided into several delay groups. When the DCO operates in high frequency, the desired delay time is short. Thus the some segmented delay groups can be disabled and the power consumption can be reduced.

Second, in order to increase the frequency resolution of DCO, the 1st fine-tuning stage and 2nd fine-tuning stage are added into the DCO design as shown in Fig.4 (b). The 1st stage is composed of eight 1st fine-tuning delay cells and each of which contains one inverter and one tri-stage inverter. These delay cells are controlled by the control signals (F1ON [0] ~ F1ON [7]). When the tri-stage inverter in 1st fine-tuning delay cell is enabled, the output signal of enabled tri-stage inverter has the hysteresis phenomenon. Thus the delay cell can achieve different delay time. Finally, in order to further increase the DCO resolution, the 2nd fine-tuning stage is added. It is composed of 32 tri-state inverters to improve the resolution. The gate capacitance of tri-state inverter is changed by the control signals (F2ON [0] ~ F2ON [31]) [5], [8]. As the gate capacitance of tri-state inverter changes, the delay of 2nd fine-tuning stage can be adjusted.

TABLE I. DCO SIMULATION RESULTS

	Best Case (ps)		Typical Case (ps)		Worst Case (ps)	
	Step	Range	Step	Range	Step	Range
Coarse-tuning	98.75		165.13		334.26	
1st. Fine-tuning	14.51	101.54	24.93	174.51	53.22	372.52
2nd. Fine-tuning	0.64	19.69	0.93	28.86	1.72	53.29

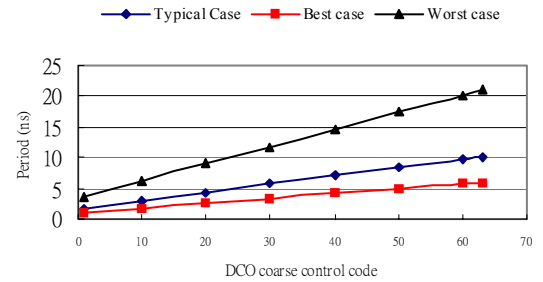


Figure 5. Linearity of DCO

TABLE II. COMPARISON WITH EXISTING DCOs

Performance Parameter	Proposed	[10]	[2]	[8]	[6]	[9]
Process	0.13 μ m CMOS	0.13 μ m CMOS	0.35 μ m CMOS	0.35 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS
Operation range (MHz)	98 ~ 599	150	152 ~ 366	18 ~ 214	413 ~ 485	140 ~ 1030
LSB resolution (ps)	0.93	40	10 ~ 150	1.55	2	22
Power consumption	110 μ W (@200MHz)	1mW (@150MHz)	NA	18mW (@200MHz)	170 ~ 340 μ W (Static only)	NA
Portability	Yes	No	Yes	Yes	No	Yes

B. The Proposed DCO Performance

Table I shows the DCO HSPICE simulation results in the typical case (TT, 0.8V, 25°C), the best case (FF, 0.88V, -40°C), and the worst case (SS, 0.72V, 125°C) respectively. Note that the controllable range of each stage should cover the step of the pervious stage. As a result, the DCO does not have any unreachable zone. It is easy to extend the controllable range of DCO by changing the coarse delay cell number. And the finest step of 2nd fine-tuning stage determines the DCO resolution. Thus the proposed DCO can achieve high resolution with 0.93ps. In addition to DCO resolution, the proposed DCO has a good linearity as shown in Fig. 5. Because DCO operates under lower supply voltage and has the segmented groups, it consumes only 110 μ W (@200MHz and fine-tuning stage providing the maximum delay). Table II lists the comparisons with the state-of-the-art DCOs. The proposed DCO has the finest resolution, the lowest power consumption, and the best portability.

V. SIMULATION RESULTS

The proposed ADPLL is designed by cell-based design flow. We use Hardware Description Language (HDL) to design and describe the proposed ADPLL. Fig.6 shows the transient response of the ADPLL, where the reference clock is 20MHz, and the division ratio (M) is 10. Thus the output frequency is 200MHz (=20MHz * 10). The TDC takes 2 reference clock cycles to complete lock-in operation and one cycle to align phase. After TDC operation is completed, the DCO control code is changed by PFD output frequency to generate desired DCO output frequency. In Fig. 6, we can see that the DCO control code will be converged to a stable value and complete the lock function.

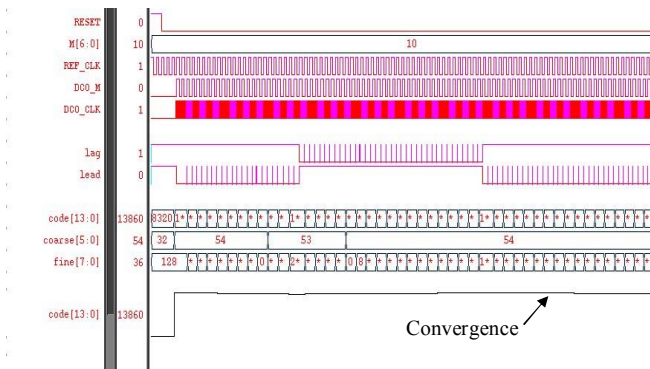


Figure 6. Transient response of the proposed ADPLL

VI. CONCLUSIONS

In this paper, a fast lock-in ADPLL has been proposed. The lock-in operation takes 2 reference clock cycles by the proposed 2-level flash TDC. In addition, a high-resolution and low-power DCO has three different tuning stages and segmented groups, resulting in 0.93ps resolution and power consumption of 110 μ W(@200MHz). Since all designs of the proposed ADPLL are described with HDL language, it can be ported to different processes, making our proposal very suitable for system-level and SoC applications.

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