Heterogeneous Platform

- Task classification & distribution
  - Control-flow tasks
    - Coordination, control, and interactive tasks
  - Dataflow tasks
    - Regular, more predictable, and highly parallel tasks

- Communication
  - Synchronization mechanism
  - Granularity

- Coprocessor design
  - Programmability
  - High speed, low power, etc

Data-dominated coprocessors with different programmability.
# Proposed DSP Platform

- # of datapaths & # of their internal parallel FUs are **scalable** to meet the performance requirements.
- The coprocessing datapaths are **configurable** for various applications based on the executing algorithms in C/C++.
- Performance boost is achieved by
  - control overheads elimination (program flow)
  - reduced load / store operations with specific SIU data generator (data generation)
  - parallel processing via SIMD-like functional units

# CASCADE – Configurable And SCAlable Dsp Environment

- The data-driven accelerators are synchronized with host’s instructions.
- The interfacing software could be compiled and scheduled (by compiler & RTOS) as usual.
Performance Improvement of MJ-like Encoder

<table>
<thead>
<tr>
<th>DCT Kernel</th>
<th>320*240 Frame</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software alone</td>
<td>5,595 Cycles</td>
</tr>
<tr>
<td>With Accelerators</td>
<td>246 Cycles</td>
</tr>
</tbody>
</table>

- The host micro-controller is 50-MHz ARM7TDMI.
- The data-driven accelerator is composed of 4 MACs.
- 8-by-8 DCT, quantization specified in JPEG standard, run-length coding, and Huffman coding are performed on the 320*240 frame.
- An ideal memory subsystem (no memory stall) is assumed for simplicity.

Conclusion

- The proposed coprocessing datapath generation is
  - easily configurable
  - performance scalable
  - simple low-power management (e.g. our example)
- The accelerating datapaths are driven by host instructions in the software interface, which is also auto-generated, to simplify the synchronization problem.
- The coprocessing datapaths boost the performance of low-cost microcontrollers to lengthen their product life span.
- Automatic generation of the accelerators with simple software-controlled interfacing dramatically reduces the development time.