VLSI Signal Processing Lab
Tay-Jyi Lin tjlin@ee.nctu.edu.tw
Department of Electronics Engineering, National Chiao Tung University

An Efficient 2-D DWT Architecture via Resource Cycling

Tay-Jyi Lin, *Chein-Wei Jen*

VLSI Signal Processing Group
Department of Electronics Engineering
National Chiao Tung University
Hsinchu, Taiwan

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Tay-Jyi Lin tjlin@ee.nctu.edu.tw
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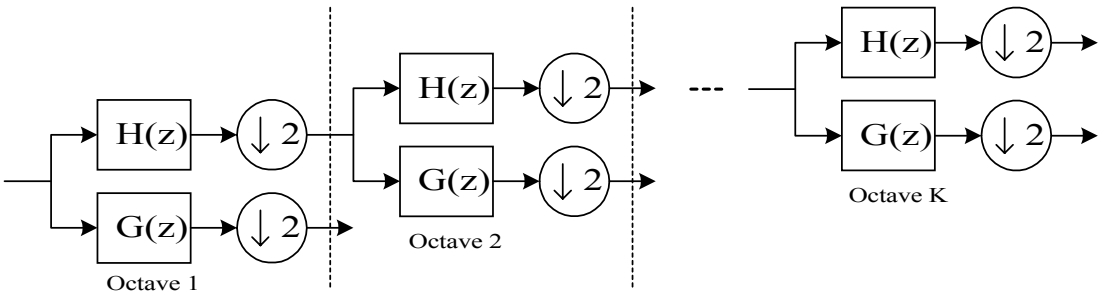
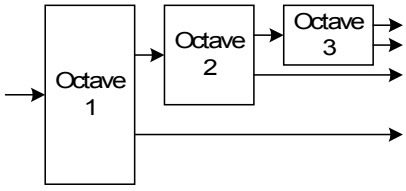
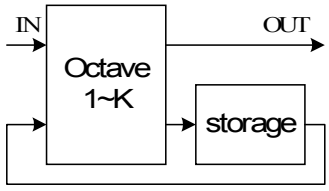
1-D DWT (Pyramid Algorithm)

- Iterative filtering with identical operations for each octave

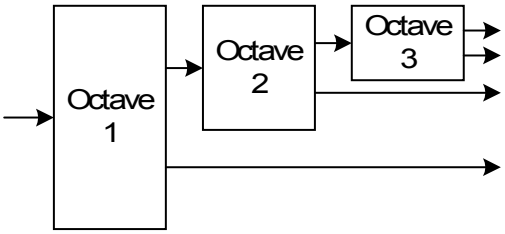


- Two alternatives can improve the hardware utilization efficiency





Intra-Octave Folding



- Folded filter architectures
  - share MACs
    (a) between H/L filters, or
    (b) among taps inside one filter
  - digit-serial filters

  e.g. 8-bit HW in octave1, 4-bit HW in octave2 and 2-bit HW in octave3, etc
- In applications with lots of decomposition levels, it is difficult to obtain all required folded architectures

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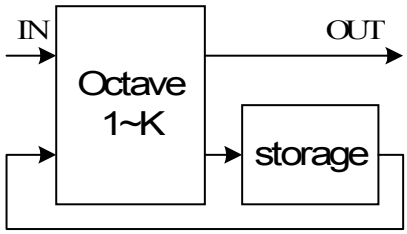
Inter-Octave Folding

Single filtering module for all octaves



- ***Blocking schedulers***
  - start an octave only when previous octave completes
  - storage size of *O(N)*
  - may require a ping-pong buffer
- ***Non-blocking schedulers***
  - interleave computations in all octaves
  - storage size of *O(KL)*
  - overheads of complex routing with very irregular data flow

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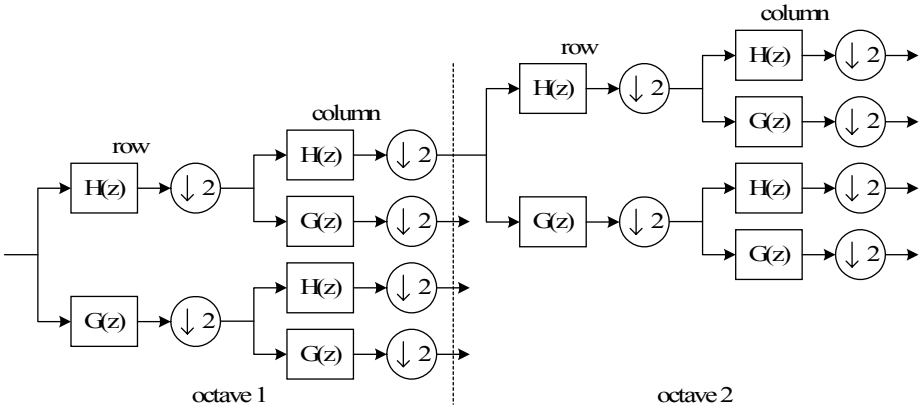
Problems in Separable 2-D DWT



- 3~6 octaves are common in practical and pure intra-octave folding is difficult → ***inter-octave folding***
- Total data rate keeps the same inside one octave → ***interleaved column filtering***
- Dynamic range & precision problems → ***resource cycling via dynamic reconfiguration***

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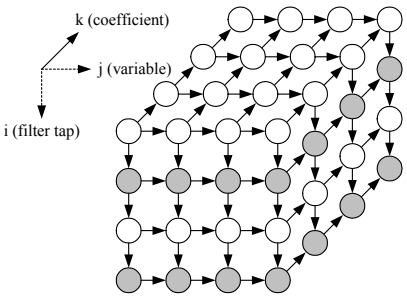
Distributed Arithmetic (DA)



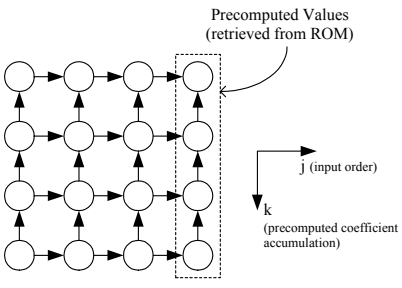
$$\sum_{i=0}^{L-1} h_i \cdot x_i = \sum_{i=0}^{L-1} h_i \cdot \left(\sum_{j=0}^{N-1} x_{i,j} \cdot 2^{-j} \right) = \sum_{j=0}^{N-1} \left(\sum_{i=0}^{L-1} h_i \cdot x_{i,j} \right) \cdot 2^{-j}$$

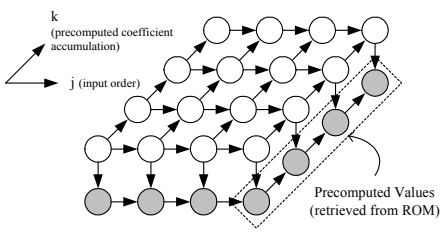
L *N*-bit MAC operations

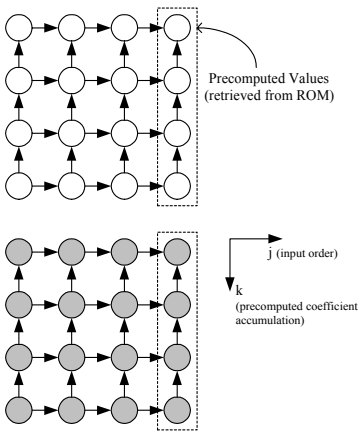
N 2^L×*N*-bit table lookup + 1 *N*-bit multiplication

(Memory-based Architecture with Scalable Wordlength)

Polyphase Decomposition







N 2×$2^{L/2}$×*N*-bit table lookup + 2 *N*-bit multiplication

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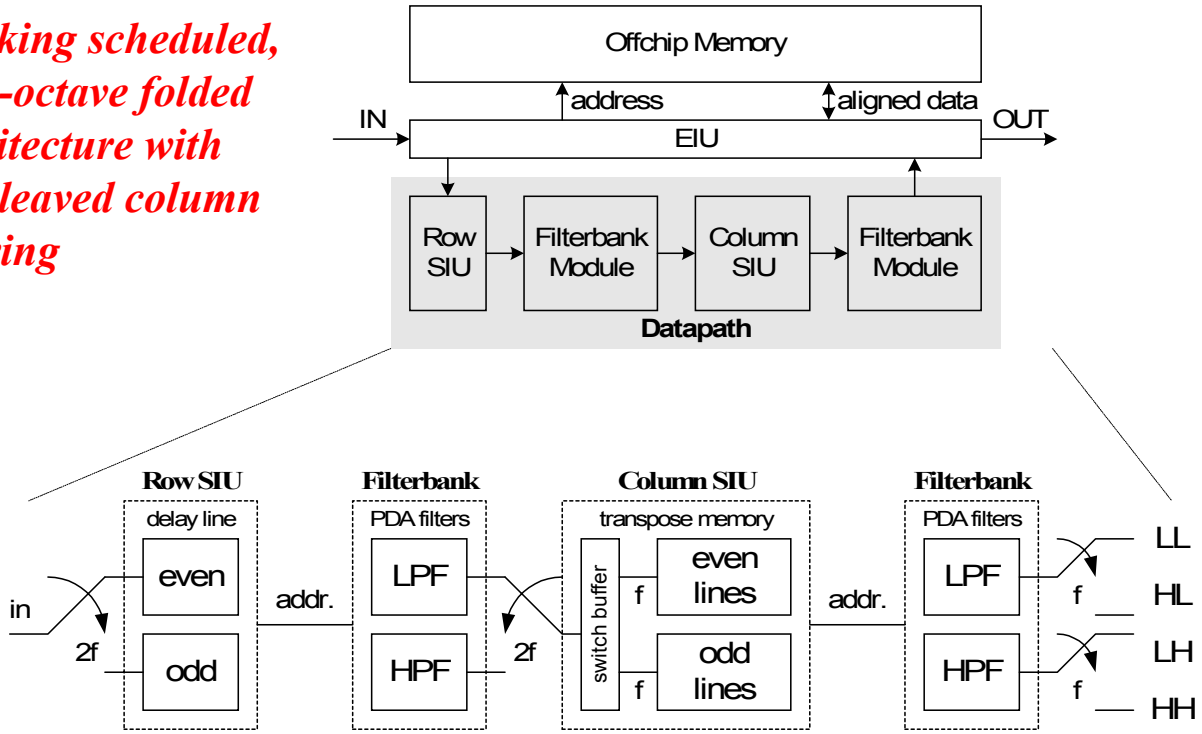
Proposed 2-D DWT Architecture

Blocking scheduled, inter-octave folded architecture with interleaved column filtering



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Fixed-Point Implementation with Full Precision

	Data Samples	Transpose Memory	Full-Precision Multiplication
1st Octave	$N \times N$	LN	$n \times m$
			$(n+m+p) \times m$
2nd Octave	$(N/2) \times (N/2)$	$LN/2$	$(n+2m+2p) \times m$
			$(n+3m+3p) \times m$
3rd Octave	$(N/4) \times (N/4)$	$LN/4$	$(n+4m+4p) \times m$
			$(n+5m+5p) \times m$

$N \times N$: image size; L: number of taps; $p = \log2\ (L)$
n: input wordlength; m: filter wordlength;

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Metamer (Reconfigurable Fabric)

- General-purpose
  - RAM
    - implements the truth table as 2-Level combinational logic (ROM)
    - pre-computed value lookup
  - FPGA & its descendants
  - reconfigurable array processors
- Application-specific
  - programmable filter length
  - fused DCT/IDCT, DWT/IDWT

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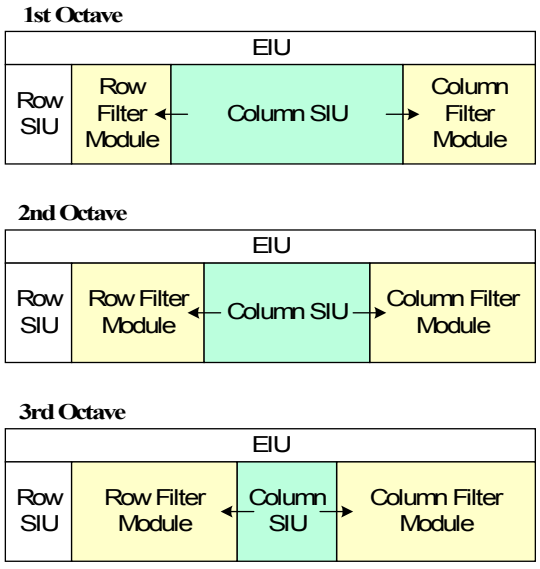
FPGA Implementation

- Wordlength increasing rate for 100% HW recycled

$$l = \frac{NL \cdot n}{NL + 8D}$$

- CRF(13,7) in JPEG-2000 & 512-by-512 image: ***l=2.4***
  i.e. ***8-bit*** & ***10-bit*** for row & column filtering respectively in the first octave; ***12-bit*** & ***14-bit*** in the second octave and ***16-bit*** & ***18-bit*** in the third octave
- Target: Xilinx XCV300PQ240-6
  Performance: 40.85MHz operation & 50MHz SelectMAP reconfiguration



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Experiment Results

	PSNR (dB)		Area
	Lena	Baboon	
8-bit	39.2899	39.3210	1.0
16-bit	87.4878	87.4892	2.0
Proposed	64.9259	64.9253	1.2

60.89 512×512 8-bit grayscale images per second (including reconfiguration overhead) into three decomposition levels.

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Conclusion

- DWT architectures
  - filtering module (computation)
  - data generation module (routing/storage)

  major problems: ***utilization***
- Resource cycling among more divergent tasks is possible via ***architecture transformation*** at design time and ***dynamic reconfiguration*** with finer granularity at run time against worst-case designs
- Future directions
  - specialized metamer design with automatic space exploration to minimize configuration overhead
  - adapted to more popular non-blocking MRPA-based architectures