Tay-Jyi Lin

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Chia-Yi 62102, Taiwan
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Professional Experiences

- ***Associate Professor*** 2016/8 ~ Present
  Assistant Professor 2010/8 ~ 2016/7
  Department of Computer Science and Information Engineering,
  National Chung Cheng University (CCU)

- ***Director*** 2016/6 ~ Present
  SoC Research Center, CCU

- ***Research Assistant Professor*** 2006/1 ~ 2010/7
  Microelectronics & Information Systems Research Center,
  National Chiao Tung University (NCTU)
  Conduct researches on Embedded Multicore and Hearing Aid Architectures

- ***Researcher & Project Manager*** 2003/3 ~ 2010/7
  SoC Technology Center (STC), Industrial Technology Research Institute (ITRI)
  Lead Processor Design Department for Parallel Architecture Core (PAC) Project

Education

- ***Ph.D. in Electronics Engineering***, NCTU, Taiwan 2005/10
  Dissertation: Microarchitecture Designs for Advanced Digital Signal Processors

- ***B.S. in Electrical & Control Engineering***, NCTU, Taiwan 1998/6

Awards and Honors

- *Young Scholar Award*, CCU 2015
- *Outstanding Chip Design Award*, National Chip Implementation Center (CIC) 2014
- *Third Prize Award*, Intelligent Electronics System Design Contest, Ministry of Education (MOE) 2014
- *Winning Prize*, Golden Silicon Award, MXIC 2013
- *Outstanding SoC Design Development Award*, Andes Technology 2012
- *Outstanding Patent Award*, ITRI 2012
- *Third Place Award*, ARM Design Contest 2012
- *Second Place Award*, Intelligent Electronics System Design Contest, MOE 2012
- *Second Place Award*, Embedded System Design Contest, MOE 2011
- *Best Paper Award*, VLSI Design/CAD Symposium 2009
- *Special Feature Award*, University LSI Design Contest, ASP-DAC 2009

- *Outstanding Design Award*, University LSI Design Contest, ASP-DAC 2006
- *First Place Award*, SIP Design Contest, MOE 2005
- *Best Paper Award*, APCCAS 2004
- *First Place Award*, SIP Design Contest, MOE 2004
- *Second Place Award*, SIP Design Contest, MOE 2003
- *First Place Award*, CPLD Design Contest, Lattice 2000

Research Interests

- Variation-resilient and ultra-low-voltage (ULV) system & architecture
- Programmable SoC with heterogeneous MPU/DSP/accelerators
- Biomedical signal processing system design & health-care applications
- Embedded software design

Technical Services

- TPC Member, *Asian Solid-State Circuits Conference* (*ASSCC*) 2014~
- TPC Member, *International Symposium on VLSI Design, Automation and Test* (*VLSI-DAT*) 2017~
- TPC Member, Computer Architecture, Embedded Systems, SoC, and VLSI/EDA, *ICS* 2012/14/16
- Judge Member, TI DSP/MCU Design Contest 2014
- Reviewer of *IEEE TVLSI*, *IEEE TCAS-I*, *IEEE TCAS-II*, *IEEE TCSVT*, *IEEE JETCAS*, *Journal of Signal Processing Systems*, *Journal of Information Science and Engineering*, *Concurrency and Computation*, …

Publications (2005~)

Journal Papers

[J1] P. H. Wang, W. C. Cheng, Y. H. Yu, T. C. Kao, C. L. Tsai, P. Y. Chang, **T. J. Lin**, J. S. Wang, and T. F. Chen, "Zero-counting and adaptive-latency cache using a voltage-guardband breakthrough for energy-efficient operations," accepted and to appear in *IEEE Transactions on Circuits and Systems – II: Express Briefs* (*SCI & EI*)

[J2] P. H. Wang, S. J. Tsai, R. Tanjung, **T. J. Lin**, J. S. Wang, and T. F. Chen, "Cross-matching caches: dynamic timing calibration and bit-level timing-failure mask caches to reduce timing discrepancies with low voltage processors," *Integration, the VLSI Journal*, vol. 54, Jun. 2016 (*SCI & EI*)

[J3] **T. J. Lin** and T. Y. Shyu, "Speculative lookahead for energy-efficient microprocessors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, Jan. 2016 (*SCI & EI*) (cited by **1***)

[J4] Y. J. Lin, C. L. Yang, C. W. Huang, **T. J. Lin**, C. W. Hsueh, and N. Chang, "System-level performance and power optimization for MPSoC – a memory access-aware approach," *ACM Transactions on Embedded Computing*, vol. 14, Jan. 2015 (*SCI & EI*) (cited by **2**)

[J5] P. Y. Chang, **T. J. Lin**, J. S. Wang, and Y. H. Yu, "A 4R/2W register file design for UDVS microprocessors in 65nm CMOS," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 59, Dec. 2012 (*SCI & EI*) (cited by **6**)

[J6] S. H. Chou, C. C. Chen, C. N. Wen, T. F. Chen, and **T. J. Lin**, "Hierarchical circuit-switched NoC for multicore video processing," *Microprocessors and Microsystems*, vol. 35, Mar. 2011 (*SCI & EI*) (cited by **5**)

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* The citation number was collected on Google Scholar (http://scholar.google.com/) on Jun. 21, 2016

[J7] Y. T. Kuo, **T. J. Lin**, and C. W. Liu, "Complexity-aware quantization and lightweight VLSI implementation of FIR filters," *EURASIP Journal on Advances in Signal Processing*, 2011 (*SCI & EI*) (cited by **5**)

[J8] C. W. Chang, **T. J. Lin**, C. J. Wu, J. K. Lee, Y. H. Chu, and A. Y. Wu, "Parallel architecture core (PAC) – the first multicore application processor SoC in Taiwan: Part I hardware architecture & software development tools," *Journal of Signal Processing Systems*, vol. 62, Mar. 2011 (*SCI & EI*) (cited by **18**)

[J9] Y. T. Kuo, **T. J. Lin**, Y. T. Li, and C. W. Liu, "Design & implementation of low-power ANSI S1.11 filter bank for digital hearing aids," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 57, July 2010 (*SCI & EI*) (cited by **47**)

[J10] **T. J. Lin**, P. C. Hsiao, S. K. Chen, Y. T. Kuo, and C. W. Liu, "Design & implementation of a high-performance & complexity-effective VLIW DSP for multimedia applications," *Journal of Signal Processing Systems*, vol. 51, Jun. 2008 (*SCI & EI*) (cited by **13**)

[J11] **T. J. Lin**, P. C. Hsiao, C. W. Liu, and C. W. Jen, "Area-efficient register organization for fully-synthesizable VLIW DSP cores," *International Journal of Electrical Engineering*, vol. 13, May 2006 (*EI*) (cited by **9**)

[J12] **T. J. Lin**, H. Y. Lin, C. M. Chao, C. W. Liu, and C. W. Jen, "A compact DSP core with static floating-point arithmetic," *Journal of VLSI Signal Processing*, vol. 42, Feb. 2006 (*SCI & EI*) (cited by **12**)

International Conference Papers

[IC1] Y. H. Ting, C. Y. Wang, Y. S. Chang, **T. J. Lin**, S. C. Chang, and J. S. Wang, "Overoptimistic voltage scaling in pre-error AVS systems and learning-based alleviation," accepted and to appear in *SOCC*, Sep. 2016

[IC2] T. Y. Shyu, B. Y. Su, **T. J. Lin**, C. Yeh, T. F. Chen, and J. S. Wang, "Variable-length VLIW encoding for code size reduction in embedded processors," accepted and to appear in *SOCC*, Sep. 2016

[IC3] B. H. Chen, P. Y. Chou, Y. B. Fang, L. K. Yong, **T. J. Lin**, and J. S. Wang, "Design of ultra-low-leakage near-threshold dynamic circuits in nano CMOS for IoT applications," accepted and to appear in *NANO*, Aug. 2016

[IC4] C. H. Kao, Z. H. Yang, C. L. Huang, Y. S. Chang, C. W. Wu, T. Y. Shyu, P. Y. Chou, **T. J. Lin**, and J. S. Wang, "Characterization of delay variations in modern FPGAs," in *Proc. VMC*, Nov. 2015

[IC5] P. Y. Chou, I. C. Wu, J. W. Lin, X. Y. Lin, T. F. Chen, **T. J. Lin**, and J. S. Wang, "Low-cost low-power droop-voltage-aware delay-fault-prevention designs for DVS caches," in *Proc. ASICON*, Nov. 2015

[IC6] P. Y. Chou, C. L. Liou, J. S. Wang, and **T. J. Lin**, "Operation-condition and timing-error collaborative monitoring for fixed-latency AVS designs," in *Proc. ICSICT*, Oct. 2014

[IC7] C. H. Huang, W. J. Chen, K. J. Chang, Y. H. Ting, K. C. Hsu, Y. F. Pan, C. C. Chen, Y. H. Chu, **T. J. Lin**, and J. S. Wang, "Low-power fixed-latency DSP accelerator with autonomous minimum energy tracking (AMET)," in *Proc. **Hot Chips***, Aug. 2014

[IC8] B. Y. Yang, C. C. Chang, and **T. J. Lin**, "Respiratory rhythm extraction for driver's drowsiness assessment," in *Proc. ARIS*, Jun. 2014

[IC9] C. Yeh, C. Y. Tsai, **T. J. Lin**, and J. I. Guo, "Maintaining color fidelity for dual-shot HDR imaging," in *Proc. ICCE-TW*, May 2014

[IC10] Y. H. Yu, P. H. Wang, T. F. Chen, **T. J. Lin**, and J. S. Wang, "Adaptive variable-latency cache management for low-voltage caches," in *Proc. FTFC*, May 2014

[IC11] B. Y. Yang, C. C. Chang, Y. H. Ting, J. W. Liao, H. L. Lin, **T. J. Lin**, C. Yeh, and J. S. Wang, "Accelerometer-based breathing signal acquisition with empirical mode decomposition," in *Proc. ICISA*, May 2014

[IC12] P. H. Wang, W. C. Cheng, Y. H. Yu, T. C. Kao, C. L. Tsai, P. Y. Chang, **T. J. Lin**, J. S. Wang, and T. F. Chen, "Variation-aware and adaptive-latency accesses for reliable low voltage caches," in *Proc. VLSI-SoC*, Oct. 2013 (cited by **2**)

[IC13] J. S. Wang, K. J. Chang, **T. J. Lin**, R. Wu, and C. Yeh, "A 0.36V, 33.3μW 18-band ANSI S1.11 1/3-octave filter bank for digital hearing aids in 40nm CMOS," in *Proc.* ***VLSIC***, Jun. 2013 (cited by **2**)

[IC14] **T. J. Lin**, C. A. Chien, P. Y. Chang, C. W. Chen, P. H. Wang, T. Y. Shyu, C. Y. Chou, S. C. Luo, J. I. Guo, T. F. Chen, C. H. Chuang, Y. H. Chu, L. C. Cheng, H. M. Su, C. Jou, M. Ieong, C. W. Wu, and J. S. Wang, "A 0.48V 0.57nJ/pixel video recording SoC in 65nm CMOS," in *Proc.* ***ISSCC***, Feb. 2013 (cited by **16**)

[IC15] S. H. Ou, C. W. Yeh, **T. J. Lin**, and C. W. Liu, "A smart stream controller for efficient implementation of streaming applications on the heterogeneous multicore processor," in *Proc. ISCAS*, May 2012

[IC16] **T. J. Lin**, Y. T. Kuo, Y. J. Tsai, T. Y. Shyu, and Y. H. Chu, "Energy-efficient RISC design with on-demand circuit-level timing speculation," in *Proc. ASP-DAC*, Jan. 2012 (cited by **1**)

[IC17] S. C. Chen, C. C. Chen, W. C. Guo, **T. J. Lin**, and C. W. Yeh, "Complexity-effective Hilbert-Huang transform (HHT) IP for embedded real-time applications," in *Proc. ASP-DAC*, Jan. 2012 (cited by **2**)

[IC18] Y. J. Lin, C. L. Yang, **T. J. Lin**, J. W. Huang, and N. Chang, "Hierarchical memory scheduling for multimedia MPSoCs," in *Proc.* ***ICCAD***, Nov. 2010 (cited by **5**)

[IC19] S. H. Ou, Y. C. Lin, **T. J. Lin**, and C. W. Liu, "Improving energy efficiency of functional units by exploiting their data-dependent latency," in *Proc. ISCAS*, May 2010

[IC20] K. C. Chang, Y. T. Kuo, **T. J. Lin**, and C. W. Liu, "Complexity-effective dynamic range compression for digital hearing aids," in *Proc. ISCAS*, May 2010 (cited by **8**)

[IC21] **T. J. Lin**, P. C. Hsiao, C. H. Lin, S. C. Kuo, C. K. Lin, Y. T. Kuo, C. W. Liu, and Y. H. Chu, "Collaborative voltage scaling with online STA and variable-latency datapath," in *Proc. GLSVLSI*, May 2010 (cited by **2**)

[IC22] C. N. Wen, S. H. Chou, T. F. Chen, and **T. J. Lin**, "RunAssert: a non-intrusive run-time assertion for parallel programs debugging," in *Proc. DATE*, Mar. 2010 (cited by **1**)

[IC23] P. C. Hsiao, C. H. Lin, K. C. Lee, and **T. J. Lin**, "Fast design space exploration for MPSoC architectures," in *Proc. ICCES*, Dec. 2009

[IC24] C. H. Chuang, C. L. Chen, P. C. Hsiao, and **T. J. Lin**, "Software development tools for streaming DSP applications," in *Proc. ISOCC*, Nov. 2009 (cited by **1**)

[IC25] C. H. Lin, P. C. Hsiao, C. H. Chuang, and **T. J. Lin**, "Fast architecture exploration with hierarchical trace simulations," in *Proc. ISOCC*, Nov. 2009

[IC26] S. K. Chen, **T. J. Lin**, and C. W. Liu, "Parallel object detection on heterogeneous multicore platforms," in *Proc. SiPS*, Oct. 2009 (cited by **10**)

[IC27] Y. T. Kuo, **T. J. Lin**, Y. T. Li, C. K. Lin, and C. W. Liu, "Ultra low-power ANSI S1.11 filter bank for digital hearing aids," in *Proc. ASP-DAC*, Jan. 2009 (***Special Feature Award***) (cited by **3**)

[IC28] T. W. Hsieh, P. C. Hsiao, C. Y. Liao, H. C. Hsieh, H. L. Lin, **T. J. Lin**, Y. H. Chu, and A. Y. Wu, "Energy-effective design & implementation of an embedded VLIW DSP," in *Proc. ISOCC*, Nov. 2008 (cited by **9**)

[IC29] Y. T. Kuo, **T. J. Lin**, Y. T. Li, C. K. Lin, and C. W. Liu, "Low-power ANSI S1.11 filter bank for digital hearing aids," in *Proc. ICSES*, Sep. 2008 (cited by **1**)

[IC30] J. A. Lin, Y. C. Tsai, **T. J. Lin**, and Y. Hsu, "Cycle stealing and channel management for on-chip networks," in *Proc. HPCC*, Sep. 2008

[IC31] Y. S. Chen and **T. J. Lin**, "Voltage emergence prevention for energy-efficient real-time task synchronization," in *Proc. CIT*, July 2008 (cited by **2**)

[IC32] Y. T. Kuo, **T. J. Lin**, W. H. Chang, Y. T. Li, C. W. Liu, and S. T. Young, "Complexity-effective auditory compensation for digital hearing aids," in *Proc. ISCAS*, May 2008 (cited by **9**)

[IC33] S. H. Ou, Y. Cho, **T. J. Lin**, and C. W. Liu, "Improving datapath utilization with composite functional units," in *Proc. ISCAS*, May 2008 (cited by **1**)

[IC34] **T. J. Lin**, C. N. Liu, S. Y. Tseng, Y. H. Chu, and A. Y. Wu, "Overview of ITRI PAC project – from VLIW DSP processor to multicore computing platform," in *Proc. VLSI-DAT*, Apr. 2008 (cited by **45**)

[IC35] S. H. Ou, **T. J. Lin**, S. S. Deng, C. H. Cho, and C. W. Liu, "Multithreaded coprocessor interface for multicore multimedia SoC," in *Proc. ASP-DAC*, Jan. 2008 (cited by **6**)

[IC36] Y. T. Kuo, **T. J. Lin**, Y. T. Lee, W. H. Chang, C. W. Liu, and S. T. Young, "Design of ANSI S1.11 filter bank for digital hearing aids," in *Proc. ICECS*, Dec. 2007 (cited by **10**)

[IC37] H. I. Yang, M. H. Chang, **T. J. Lin**, S. H. Ou, S. S. Deng, C. W. Liu, and W. Hwang, "A controllable low-power dual-port embedded SRAM for DSP processor," in *Proc. MTDT*, Dec. 2007 (cited by **4**)

[IC38] S. K. Chen, B. S. Wang, **T. J. Lin**, and C. W. Liu, "Rapid C to FPGA prototyping with multithreaded emulation engine," in *Proc. ISCAS*, May 2007

[IC39] P. C. Hsiao, **T. J. Lin**, C. W. Liu, and C. W. Jen, "Latency-tolerant virtual cluster architecture for VLIW DSP," in *Proc. ISCAS*, May 2007

[IC40] L. C. Lin, S. H. Ou, **T. J. Lin**, S. S. Deng, and C. W. Liu, "Single-issue 1500MIPS embedded DSP with ultra compact codes," in *Proc. ASP-DAC*, Jan. 2007

[IC41] Y. T. Kuo, **T. J. Lin**, Yi Cho, C. W. Liu, and C. W. Jen, "Programmable FIR filter with adder-based computing engine," in *Proc. ISCAS*, May 2006

[IC42] S. H. Ou, **T. J. Lin**, C. W. Huang, Y. T. Kuo, C. M. Chao, C. W. Liu, and C. W. Jen, "A 52mW 1200MIPS compact DSP for multi-core media SoC," in *Proc. ASP-DAC*, Jan. 2006 (***Outstanding Design Award***) (cited by **1**)

[IC43] C. H. Liu, **T. J. Lin**, C. W. Liu, and C. W. Jen, "On-demand pipelining for improving energy-awareness," in *Proc. ASSCC*, Nov. 2005

[IC44] Y. T. Kuo, **T. J. Lin**, C. W. Liu, and C. W. Jen, "Architecture for area-efficient 2-D transform in H.264/AVC," in *Proc. ICME*, July 2005 (cited by **8**)

[IC45] W. S. Huang, **T. J. Lin**, S. H. Ou, C. W. Liu, and C. W. Jen, "Pipelining technique for energy-aware datapaths," in *Proc. ISCAS*, May 2005 (cited by **3**)

[IC46] C. H. Liu, **T. J. Lin**, C. M. Chao, P. C. Hsiao, L. C. Lin, S. K. Chen, C. W. Huang, C. W. Liu, and C. W. Jen, "Hierarchical instruction encoding for VLIW digital signal processors," in *Proc. ISCAS*, May 2005 (cited by **8**)

[IC47] **T. J. Lin**, C. C. Lee, C. W. Liu, and C. W. Jen, "A novel register organization for VLIW digital signal processors," in *Proc. VLSI-TSA-DAT*, Apr. 2005 (cited by **15**)

[IC48] S. H. Ou, **T. J. Lin**, H. Y. Lin, C. M. Chao, C. W. Liu, and C. W. Jen, "Lightweight arithmetic units for VLSI digital signal processors," in *Proc. VLSI-TSA-DAT*, Apr. 2005 (cited by **1**)

[IC49] **T. J. Lin**, C. M. Chao, C. H. Liu, P. C. Hsiao, S. K. Chen, L. C. Lin, C. W. Liu, and C. W. Jen, "A unified processor architecture for RISC & VLIW DSP," in *Proc. GLSVLSI*, Apr. 2005 (cited by **23**)

Domestic Conference Papers

[DC1] Y. J. Lin, C. L. Yang, J. W. Huang, **T. J. Lin**, and N. Chang, "Memory access aware power gating for MPSoCs," in *Proc. VLSI Design/CAD*, Aug. 2011

[DC2] S. C. Chuang, Y. L. Liu, S. H. Chou, S. C. Kuo, K. J. Chang, **T. J. Lin**, T. F. Chen, and C. N. Wen, "Design and analysis of adaptive pipeline for ultra-low voltage microprocessors," in *Proc. VLSI Design/CAD*, Aug. 2010

[DC3] Y. J. Lin, J. W. Huang, C. L. Yang, **T. J. Lin**, and N. Chang, "Hierarchical memory scheduling for multimedia MPSoCs," in *Proc. VLSI Design/CAD*, Aug. 2010

[DC4] M. H. Chuang, Y. T. Kuo, K. C. Chang, **T. J. Lin**, and C. W. Liu, "Quasi-ANSI S1.11 1/3-octave filter bank for digital hearing aids," in *Proc. VLSI Design/CAD*, Aug. 2010

[DC5] X. C. Wu, Y. J. Lin, P. J. Huang, **T. J. Lin**, and C. L. Yang, "Instruction-level power estimation for embedded VLIW digital signal processors," in *Proc. VLSI Design/CAD*, Aug. 2009 (***Best Paper Award***)

[DC6] J. A. Lin, Y. C. Tsai, **T. J. Lin**, and Y. Hsu, "Cycle stealing buffers and physical channel management scheme for wormhole-based on-chip networks," in *Proc. NCS*, Dec. 2007

[DC7] S. H. Ou, L. C. Lin, **T. J. Lin**, S. S. Deng, P. H. Wang, Y. Cho, C. C. Chen, and C. W. Liu, "A compact 300MHz/1500MIPS DSP with improved single-issue unit," in *Proc. VLSI Design/CAD*, Aug. 2006

[DC8] C. M. Chao, **T. J. Lin**, C. W. Liu, and C. W. Jen, "A simple & effective method for compiling high-level languages into application-specific processor architectures," in *Proc. VLSI Design/CAD*, Aug. 2005

[DC9] P. C. Hsiao, **T. J. Lin**, C. W. Liu, and C. W. Jen, "Efficient datapath design for pipelined & clustered DSP processors," in *Proc. VLSI Design/CAD*, Aug. 2005

Patents

項次	專利國	專利號	專利名稱	發明人
1	US	9,064,153	Video device for realtime pedaling frequency estimation	林泰吉、葉經緯、苗淵翔、唐韶謙
2	US	8,972,699	Multicore interface with dynamic task management capability and task loading/offloading method thereof	林泰吉、謝天威、朱元華、歐士豪、鄧翔升、劉志尉
	中華民國	I386814	具有動態工作管理能力的多處理器界面及其程序加載或卸載方法	
3	US	8,589,718	Performance scaling device, processor having the same, and performance scaling method thereof	林騏宏、蕭丕承、林泰吉、馬金溝
	中華民國	I423017	效能調整裝置、具有此效能調整裝置的處理器及其效能調整方法	
4	US	8,499,188	Processing device for determining whether to output a first data using a first clock signal or a second data using delay from the first clock signal according to a control signal	林周坤、林泰吉、蕭丕承、朱元華
5	US	7,877,741	Method and corresponding apparatus for compiling high-level languages into specific processor architectures	林泰吉、趙至敏、劉志尉、任建葳、廖宜道、黃柏涵
	中華民國	I306215	高階語言編譯方法及裝置	
6	US	7,406,588	Dynamically reconfigurable stages pipelined datapath with data valid signal controlled multiplexer	林泰吉、劉志尉、任建葳、黃柏涵、黃維聖、張展豪
	中華民國	I259659	可動態調變級數之管線化資料路徑	
7	US	7,404,048	Inter-cluster communication module using the memory access network	林泰吉、蕭丕承、劉志尉、任建葳、廖宜道、黃柏涵
	中華民國	I283411	使用記憶體存取網路之叢集連結模組	
8	中華民國	申請中	呼吸訊號擷取方法及其擷取裝置	林泰吉、楊博元、丁意軒、葉經緯
	US	申請中	Method and device for retrieving a breathing signal	
9	中華民國	申請中	結合抖動偵錯的前瞻臆測處理系統及其處理方法	林泰吉、林泓志、許庭瑜、王進賢
	US	申請中		
10	中華民國	申請中	應用於可變延遲管線設計之前瞻臆測機置	林泰吉、王進賢、許庭瑜、丁意軒
	US	申請中	Speculative lookahead processing device and method	
11	中華民國	申請中	自適電壓調整系統	林泰吉、蕭丕承
	US	申請中	Adaptive voltage scaling system	
12	中華民國	I334990	虛擬叢集架構與方法	林泰吉、任建葳、蕭丕承、林禮圳、劉志尉
	US	申請中	Virtual cluster architecture	
13	中華民國	I318359	整合式單核心、多模式處理器及其指令執行方法	林泰吉、任建葳、劉佳憲、劉志尉、廖宜道、黃柏涵
14	中華民國	I275994	超長指令集數位訊號處理器之指令編碼及其解碼方法	李則暉、廖宜道、林泰吉、劉明倫
15	中華民國	I266238	適用於超長指令字元之階層式指令編碼方法及其解碼器	任建葳、林泰吉、張金祺、趙至敏、劉志尉
16	中華民國	I258698	適用於嵌入式數位訊號處理之靜態浮點運算單元及其移位控制方法	林泰吉、林宏曄、任建葳、劉志尉、廖宜道
17	中華民國	I227404	使用暫存器置換之叢集通訊方法	任建葳、林泰吉、張金祺、李承家、劉志尉
18	中華民國	申請中	多工處理器及其任務切換方法	林泰吉、黃保瑞、劉志尉、陳信凱、王炳勛
	US	申請中	Lightweight context switch mechanism for embedded multitasking processors	