

Curriculum Vitae

Pao-Ann Hsiung

September 10, 2018

Contents

1	Short Biography	1
2	Personal Information	2
3	Education	2
4	Professional Memberships	2
5	Professional Listings	2
6	Academic Employment	4
7	Courses Taught	5
8	Research Interests	5
9	Honors and Awards	6
10	Publication List	8
	(A) International Journal Papers	8
	(B) Books and Chapters	13
	(C) International Conference Papers	14
	(D) Local Conference Papers	27
	(E) Technical Reports and Others	30
11	Tool and Software Developments	32
12	Invited Tutorials and Short Courses	33
13	Invited Talks	34
14	Journal Editorships	37
	14.1 Editorial Board Member of several journals	37
	14.2 Guest Editing Journal Special Issues	38
15	Conference Program Committee Member	39
16	Conference Organization and Chairing	50
17	Students Advised	53
	17.1 Doctoral Students	53
	17.2 Master Students	54
18	Research Grants	60
	18.1 Research Project Grants	60
	18.2 Construction Project Grants	61
	18.3 Educational Reform Project Grants	61

18.4 Workshop Organization Grant	62
18.5 Travel Grants	62
18.6 Speaker Grants	63
19 Paper Refereeing	63
19.1 International Conferences	63
19.2 International Journals	64

1 Short Biography

Pao-Ann Hsiung, *Ph.D.*, received his B.S. in Mathematics and his Ph.D. in Electrical Engineering from the National Taiwan University, Taipei, Taiwan, ROC, in 1991 and 1996, respectively. From 1996 to 2000, he was a post-doctoral researcher at the Institute of Information Science, Academia Sinica, Taipei, Taiwan, ROC. From February 2001 to July 2002, he was an assistant professor and from August 2002 to July 2007 he was an associate professor in the Department of Computer Science and Information Engineering, National Chung Cheng University, Chiayi, Taiwan, ROC. Since August 2007, he has been a full professor. From May 2008 to July 2011, he was the division chief of the division of information management, computer centre, National Chung Cheng University. From August 2011 to January 2016, he has been the department chair. From February 2016 to July 2017, he was the Dean of International Affairs at the National Chung Cheng University.

Dr. Hsiung has published more than 250 papers in international journals and conferences. He was the recipient of the 2010 Outstanding Research Award given by the National Chung Cheng University to three faculty members only. He received the 2001 ACM Taipei Chapter Kuo-Ting Li Young Researcher for his significant contributions to design automation of electronic systems. He was also a recipient of the 2004 Young Scholar Research Award given by National Chung Cheng University to five young faculty members per year. He received several advisor awards for Best Master Theses, embedded system competitions, and RFID design competitions.

Dr. Hsiung is a fellow of the IET, a senior member of the IEEE, a senior member of the ACM, and a life member of the IICM. He has been included in several professional listings such as Marquis' Who's Who in the World, Marquis' Who's Who in Asia, Outstanding People of the 20th Century by International Biographical Centre, Cambridge, England, Rifacimento International's Admirable Asian Achievers (2006), Afro/Asian Who's Who, and Asia/Pacific Who's Who. Dr. Hsiung is the editor-in-chief for the software engineering topic of the *International Journal of Advancements in Computing Technology* (IJACT), Advanced Institute of Convergence IT, and the editor-in-chief for the automated control systems topic of the *International Journal of Intelligent Information Processing* (IJIIP), Human and Sciences Publication, since 2011. He is an editor of *The Scientific World Journal* (TSWJ), Hindawi Publishing Corporation, since 2012. He is also an editor for the *International Journal of Next Generation Information Technology* (JNIT), Human and Sciences Publication, the *International Journal of Advances in Information Sciences and Service Sciences* (AISS), Advanced Institute of Convergence IT, the *International Journal of Advancements in Computing Technology* (IJACT), Advanced Institute of Convergence IT, Korea; the *International Journal of Embedded Systems* (IJES), Inderscience Publishers, USA; the *International Journal of Multimedia and Ubiquitous Engineering* (IJMUE), Science and Engineering Research Center (SERSC), USA; an associate editor of the *Journal of Software Engineering* (JSE), Academic Journals, Inc., USA; an editorial board member of the *Open Computer Science Journal*, Bentham Science Publishers, Ltd., USA; an international editorial board member of the *International Journal of Patterns* (IJOP). Dr. Hsiung has been on the program committee of more than 130 international conferences. He served as organizer, program chair, steering committee member for RTC'99, DSVV'2000, PDES'2005, WoRMES'2009, ITNG'2010, ITNG'2011, ERSA'2011, ATVA'2011, FPT'2012, HMC'2013, ePaMuS'2013, MCSoc'2013, HP3C'2014. He has taken an active part in paper refereeing for international journals and conferences.

Dr. Hsiung's main research interests include reconfigurable computing and system design, multi-core programming, smart city technology such as smart traffic and smart grid, cognitive radio architecture, System-on-Chip design and verification, embedded software synthesis and verification, real-time system design and verification, hardware-software codesign and coverification, and component-based object-oriented application frameworks for real-time embedded systems.

2 Personal Information

Name Pao-Ann Hsiung
Sex Male
Date of birth January 1, 1967
Citizenship Republic of China
Address Department of Computer Science and Information Engineering
National Chung Cheng University
168, University Road, Min-Hsiung
Chiayi-62102, Taiwan, ROC.
Telephone +886-5-2720411 ext. 23100 or 33119 (Office)
Fax +886-5-2720859
E-mail hpa@computer.org, pahsiung@cs.ccu.edu.tw, pahsiung@gmail.com
URL <http://www.cs.ccu.edu.tw/~pahsiung/>

3 Education

Sept. 1992 – July 1996 **Ph.D.** Graduate Institute of Electrical Engineering,
National Taiwan University, Taipei, TAIWAN.
Sept. 1991 – July 1992 **Master** Graduate Institute of Electrical Engineering,
National Taiwan University, Taipei, TAIWAN.
(direct doctorate after 1 year)
Sept. 1987 – June 1991 **B.S.** Department of Mathematics,
National Taiwan University, Taipei, TAIWAN.

4 Professional Memberships

1. Fellow, IET (The Institution of Engineering and Technology), UK,
2. Senior Member, IEEE (The Institute of Electrical and Electronics Engineers), USA,
3. Senior Member, ACM (Association of Computing Machinery), USA, and
4. Life Member, IICM (Institute of Information and Computing Machinery), Taiwan.

5 Professional Listings

Dr. Hsiung has been either invited for inclusion or automatically included in the following professional listings.

1. *Marquis' Who's Who in the World*, since the 17th Millenium Edition, 2000.
“<http://www.marquiswhoswho.com/>”
2. *Marquis' Who's Who in Asia*, 1st Edition, 2007.
“<http://www.marquiswhoswho.com/>”

3. *Outstanding People of the 20th Century*,
Second Edition, 2000, International Biographical Centre, Cambridge, England.
4. *Outstanding People of the 21st Century*,
First Edition, 2008, International Biographical Centre, Cambridge, England.
5. *Admirable Asian Achievers*,
First Edition, 2006, Rifacimento International, India.
6. *Afro/Asian Who's Who*, Volume 1, 2007, Rifacimento International, India.
7. *Asia/Pacific Who's Who*, Volume VII, 2007, Rifacimento International, India.
8. *Who's Who in Formal Methods*
“<http://www.comlab.ox.ac.uk/archive/formal-methods/whos-who.html>”
9. *SIGACT TCS Virtual Address Book of Theoretical Computer Scientists*
“<http://sigact.acm.org/tcs-address/woody.html>”
10. *HPSearch: Home Pages of Computer Scientists*
“<http://pranger.uni-trier.de/hp/a-tree/141.html>”
11. *Home Pages of researchers in semantics, proofs and abstract interpretation*
“<http://www.di.ens.fr/cousot/researchers.shtml>”

6 Academic Employment

February 2016 – July 2017	Dean, International Affairs, National Chung Cheng University, Chiayi, Taiwan, R.O.C.
May 2015 – January 2016	Vice Dean, College of Engineering, National Chung Cheng University, Chiayi, Taiwan, R.O.C.
August 2011 – January 2016	Department Chair, Department of Computer Science and Information Engineering, National Chung Cheng University, Chiayi, Taiwan, R.O.C.
May 2008 – July 2011	Division Chief, Division of Information Management, Computer Center, National Chung Cheng University, Chiayi, Taiwan, R.O.C.
August 2007 – present	Professor, Department of Computer Science and Information Engineering, National Chung Cheng University, Chiayi, Taiwan, R.O.C.
August 2002 – July 2007	Associate Professor, Department of Computer Science and Information Engineering, National Chung Cheng University, Chiayi, Taiwan, R.O.C.
February 2001 – July 2002	Assistant Professor, Department of Computer Science and Information Engineering, National Chung Cheng University, Chiayi, Taiwan, R.O.C.
October 1996 – January 2001	Postdoctoral Fellow, Institute of Information Science, Academia Sinica, Taipei, Taiwan, R.O.C.
August 1993 – July 1996	Teaching Assistant and System Manager, Department of Mathematics, National Taiwan University, Taipei, Taiwan, R.O.C.

7 Courses Taught

Graduate Level		Undergraduate Level	
Course Name	Semester	Course Name	Semester
Introduction to Deep Learning	'18S		
R Programming	'15S		
RFID System and Appl.	'13F, 15'F, 17'F		
Operating System	'08-'10F		
Reconfigurable Computing	'07S,'08S	Software Engineering	'05-'16F
Embedded Software Design	'02S,'04S,'05F, '06F, '09-'11S	System Programming	'05-'12S
Computer-Aided Verification	'01F,'04S,'06S	Operating System	'01-'04F
SoC Design Flow and Tools	'03F,'05S	Program Design	'02-'03S,
Software Engineering	'03S,'07S, '08-'10F, '12-'18F	Intro. to Comp. Sci.	'01S
Hardware-Software Co-design	'01S	Fund. of Comp. Sci.	'11-'15F
		CS Seminar	'12-'16S

S: Spring, F: Fall

8 Research Interests

Applications	Precision Agriculture, Smart Traffic, Smart Grid, Landslide Prediction, Driver Fatigue Predictions
Theory	Formal Verification of Concurrent Real-Time Systems, Formal Verification/Design of Safety-Critical Systems, Hardware-Software and SoC Coverification,
Hardware/Software	Codesign Methodology for Embedded Systems and SoC, Reconfigurable Systems and SoC, Coverification Techniques,
System Design	System-Level Design Automation, Multiprocessor Architecture Design, Smart Grid System Design Smart Traffic System Design
Software	Multi-core Programming for Embedded Systems, Embedded Software Synthesis, Model-Checking Tool Development, Real-Time Application Development, Object-Oriented Application Framework Design
Communication	Reasoning and Learning in Cognitive Radios Low-Power Wide-Area Networking (LPWAN) such as LoRa, NB-IoT, etc.

9 Honors and Awards

- *2010 Outstanding Research Award*, National Chung Cheng University, (three faculty members awarded in 2010).
- *2004 Young Scholar Research Award*, National Chung Cheng University, (four faculty members awarded in 2004, NT\$400,000 research fund and NT\$60,000 cash awarded to each person).
- *2001 Kuo-Ting Li Young Researcher Award*, sponsored by the *ACM Taipei Chapter* and the *Institute of Information and Computing Machinery*, 2001 (one recipient in the whole country per year).
- *Advisor of one of the best Master Thesis in Computer Science*, Student: Feng-Shi Su, Thesis Title: “Formal Synthesis and Code Generation of Embedded Software Using Extended Quasi-Static Scheduling,” Dept of Computer Science and Information Engineering, National Chung Cheng University, June 2002, awarded by the *Institute of Information and Computing Machinery*, 2002.
- *Advisor of one of the best Master Thesis in Computer Science*, Student: Cheng-Yi Lin, Thesis Title: “Quasi-Dynamic Scheduling for the Synthesis of Real-Time Embedded Software with Local and Global Deadlines,” Dept of Computer Science and Information Engineering, National Chung Cheng University, July 2003, awarded by the *Institute of Information and Computing Machinery*, 2003.
- *Advisor of one of the best Master Thesis in Computer Science*, Student: Wen-Hsiu Liao, Thesis Title: “Infrastructure of a Formal Verification Platform for SoC,” Dept of Computer Science and Information Engineering, National Chung Cheng University, July 2004, awarded by the *Institute of Information and Computing Machinery*, 2004.
- *Advisor of one of the best Master Thesis in Computer Science*, Student: Chih-Hao Tseng, Thesis Title: “UML-Based Rapid Prototyping Design Flow for Dynamically Reconfigurable Computing Systems,” Dept of Computer Science and Information Engineering, National Chung Cheng University, July 2005, awarded by the *Institute of Information and Computing Machinery*, 2005.
- *Contest Winning Team Advisor Award*, Third Prize, National Contest on Embedded Software Design, sponsored by the Ministry of Education, Taiwan, 2005, (Title: RFID: Airport Luggage Automation, Members: Chien Rong-Yin, Wu Cheng-Yang, and Lin Gen-Hsien)
- *Advisor of one of the best Master Thesis in Computer Science*, Student: Yean-Ru Chen, Thesis Title: “Automatic Failure Analysis using Extended Safecharts,” Dept of Computer Science and Information Engineering, National Chung Cheng University, July 2006, awarded by the *Institute of Information and Computing Machinery*, 2006 (acceptance rate: 12%).
- *Advisor of one of the best Master Thesis in Computer Science*, Student: Hsian-Win Liao, Thesis Title: “Multi-Objective Placement of Reconfigurable Hardware Tasks in Real-Time Systems,” Dept of Computer Science and Information Engineering, National Chung Cheng University, July 2007, awarded by the *Institute of Information and Computing Machinery*, 2007.

- *Advisor of one of the best Master Thesis in Computer Science*, Student: Kuo-Cherng Chiang, Thesis Title: “Predictable and Adaptive Reconfigurable Network-on-Chip,” Dept of Computer Science and Information Engineering, National Chung Cheng University, July 2008, awarded by the *Institute of Information and Computing Machinery*, 2008.
- *Advisor of one of the best Master Thesis in Computer Science*, Student: Wei-Wen Lin, Thesis Title: “An Efficient Hardware/Software Communication Mechanism for Reconfigurable Network-on-Chip,” Dept of Computer Science and Information Engineering, National Chung Cheng University, July 2009, awarded by the *Institute of Information and Computing Machinery*, 2009. (acceptance rate: $23/133 = 17.3\%$)
- *Advisor of one of the best Master Thesis in Computer Science*, Student: Shih-Shen Lu, Thesis Title: “Congestion- and Energy-Aware Run-time Task Mapping for Network-on-Chip Architecture,” Dept of Computer Science and Information Engineering, National Chung Cheng University, July 2010, awarded by the *Institute of Information and Computing Machinery*, 2010.
- *Contest Winning Team Advisor Award*, Third Prize, RFID Tendency Cup, sponsored by the Ministry of Economics and Ministry of Education, Taiwan, 2007 (Title: RFID-based R-Generation Postal System, Members: Li Shih-Chiang, Chiu Meng-Chieh, and Hsu Chi-Ying)
- *Contest Winning Team Advisor Award*, Second Prize, Hardware-Software Integration Group, National Contest on Embedded System Design, sponsored by the Ministry of Education, Taiwan, 2008, (Title: UML-based Hardware-Software Codesign Platform for Dynamically Partially Reconfigurable Network Security Systems, Members: Chun-Hsian Huang, Kenshing Huang, Chun-Ting Lan)
- *Contest Winning Team Advisor Award*, Third Prize, Hardware-Software Integration Group, National Contest on Embedded System Design, sponsored by the Ministry of Education, Taiwan, 2009, (Title: Hierarchical Operating System Model for Dynamically Self-Reconfigurable Systems, Member: Chun-Hsian Huang)
- *Contest Winning Team Advisor Award*, Third Prize, Hardware-Software Integration Group, National Contest on Embedded System Design, sponsored by the Ministry of Education, Taiwan, 2009, (Title: Reliable and Power-Aware Reconfigurable Network-on-Chip with Operating System Management, Member: Jih-Sheng Shen)
- *Contest Winning Team Advisor Award*, Merit Award, 3G Mobile Campus Group, National Contest on Telecommunication Value-Added Application, Taiwan November 2009, (Title: RFID 3G Mobile Campus Network, Group Leader: Shih-Shen Lu)
- *Best Paper Award*, C.-H. Huang, J.-S. Shen, and P.-A. Hsiung, “Model-Based Verification and Estimation Framework for Dynamically Partially Reconfigurable System,” National Computer Symposium, Workshop on Computer Architecture, Embedded Systems, and VLSI/EDA, Taiwan, December 2009.
- *Best Paper Award*, J.-S. Shen, C.-H. Huang, and P.-A. Hsiung, “PRESSNoC: Power-Aware and Reliable Encoding Schemes Supported Reconfigurable Network-

on-Chip Architecture,” Fourth International Conference on Embedded and Multimedia Computing (EM-Com), Jeju, Korea, December 2009.

- *Contest Winning Team Advisor Award*, Finalist Award, National Yi-Shiou University U-RFID Contest, Kaoshiung, Taiwan, October 2010, (Title: The RFID Generation – Mobile RFID Technology for Outdoor Teaching, Members: Shu-Hwa Hwang, Ching-Chun Hwang, and Sheng-Wen Chen)
- *Contest Winning Team Advisor Award*, Merit Award, National RFID Design and Application Contest, Ming-Hsin University of Science and Technology, Taiwan, December 2010, (Title: Mobile RFID Technology for Outdoor Teaching, Members: Shu-Hwa Hwang, Ching-Chun Hwang, and Sheng-Wen Chen)
- *Creative Innovation Award*, Y.-R. Chen, P.-C. Hsieh, and P.-A. Hsiung, “Timing Optimization and Control for Smart Traffic,” Chiuan-Yan Technology Thesis Award (CYTTA), Kenting, Taiwan, November 2014.
- *Creative Innovation Award*, W.-H. Wu, C.-C. Tsai, H.-L. Chao, and P.-A. Hsiung, “Micro-grid Design Modeling and Prototyping,” Chiuan-Yan Technology Thesis Award (CYTTA), Kenting, Taiwan, November 2014.

10 Publication List

(A) International Journal Papers

- [1] **P.-A. Hsiung**, S.-J. Chen, T.-C. Hu, and S.-C. Wang, “PSM: An Object-Oriented Synthesis Approach to Multiprocessor System Design,” *IEEE Transactions on VLSI Systems*, Vol. 4, No. 1, pp. 83-97, March 1996. (SCI)
- [2] **P.-A. Hsiung**, T.-Y. Lee, and S.-J. Chen, “MOBnet: An Extended Petri Net Model for the Distributed Object-oriented System-level Synthesis of Multiprocessor Systems,” *IEICE Transactions on Information and Systems*, Vol. E80-D, No. 2, pp. 232–242, February 1997. (SCI)
- [3] **P.-A. Hsiung**, C.-H. Chen, T.-Y. Lee, and S.-J. Chen, “ICOS: An Intelligent Concurrent Object-Oriented Synthesis Methodology for Multiprocessor Systems,” *ACM Transactions on Design Automation of Electronic Systems*, Vol. 3, No. 2, pp. 109–135, April 1998. (SCI)
- [4] **P.-A. Hsiung**, “CMAPS: A Cosynthesis Methodology for Application-Oriented Parallel Systems,” *ACM Transactions on Design Automation of Electronic Systems*, Vol. 5, No. 1, pp. 51–81, January 2000. (SCI)
- [5] **P.-A. Hsiung**, “Hardware-Software Timing Coverification of Concurrent Embedded Real-Time Systems,” *IEE Proceedings on Computers and Digital Techniques*, Vol. 147, No. 2, pp. 81–90, March 2000. (SCI)
- [6] J.-M. Fu, T.-Y. Lee, **P.-A. Hsiung**, and S.-J. Chen, “Hardware-Software Timing Coverification of Distributed Embedded Systems,” *IEICE Transactions on Information and Systems*, Vol. E83-D, No. 9, pp. 1731–1740, September 2000. (SCI)

- [7] **P.-A. Hsiung**, “Embedded Software Verification in Hardware-Software Codesign,” *Journal of Systems Architecture — the Euromicro Journal*, Vol. 46, No. 15, pp. 1435–1450, Elsevier Science, the Netherlands, December 2000. (SCI)
- [8] **P.-A. Hsiung**, “POSE: A Parallel Object-Oriented Synthesis Environment,” *ACM Transactions on Design Automation of Electronic Systems*, Vol. 6, No. 1, pp. 67–92, January 2001. (SCI)
- [9] T.-Y. Lee, **P.-A. Hsiung**, and S.-J. Chen, “Hardware-Software Multi-Level Partitioning for Distributed Embedded Multiprocessor Systems,” *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, Vol. E48-A, No. 2, pp. 614–626, February 2001. (SCI)
- [10] T.-Y. Lee, **P.-A. Hsiung**, and S.-J. Chen, “DESC: A Hardware-Software Codesign Methodology for Distributed Embedded Systems,” *IEICE Transactions on Information and Systems* Vol. E84-D, No. 3, pp. 326–339, March 2001. (SCI)
- [11] F. Wang and **P.-A. Hsiung**, “Efficient and User-Friendly Verification,” *IEEE Transactions on Computers*, Vol. 51, No. 1, pp. 61–83, January 2002. (SCI)
- [12] T.-Y. Lee and **P.-A. Hsiung**, “Embedded Software Synthesis and Prototyping,” *IEEE Transactions on Consumer Electronics*, Vol. 50, No. 1, pp. 386–392, February 2004. (SCI)
- [13] **P.-A. Hsiung**, S.-W. Lin, C.-H. Tseng, T.-Y. Lee, J.-M. Fu, and W.-B. See, “VERTAF: An Application Framework for the Design and Verification of Embedded Real-Time Software,” *IEEE Transactions on Software Engineering*, Vol. 30, No. 10, pp. 656–674, October 2004. (SCI)
- [14] **P.-A. Hsiung**, T.-Y. Lee, J.-M. Fu, and W.-B. See, “Formal Verification of Real-Time Embedded Software in an Object-Oriented Application Framework,” *IEE Proceedings — Computers and Digital Techniques*, Vol. 151, No. 6, pp. 417–434, November 2004. (SCI)
- [15] **P.-A. Hsiung**, “Synthesis and Control of Soft Embedded Real-Time Systems,” *Annual Review of Communications*, International Engineering Consortium, USA, Vol. 57, November 2004.
- [16] **P.-A. Hsiung** and H.-C. Kao, “Device-Centric Low-Power Scheduling for Real-Time Embedded Systems,” *International Journal of Software Engineering and Knowledge Engineering (IJSEKE)*, Vol. 15, No. 2, pp. 461–466, World Scientific Publishing, Singapore, April 2005. (SCI)
- [17] **P.-A. Hsiung**, T.-Y. Lee, J.-M. Fu, and W.-B. See, “SESAG: An Object-Oriented Application Framework for Real-Time Systems,” *Software Practice and Experience*, Vol. 35, No. 10, pp. 899–921, John Wiley & Sons, August 2005. (SCI)
- [18] C.-H. Huang, S.-S. Chang, and **P.-A. Hsiung**, “Generic Wrapper Design for Dynamic Swappable Hardware IP in Partially Reconfigurable Systems,” *International Journal of Electrical Engineering*, Vol. 14, No. 3, pp. 229–238, June 2007. (EI)

- [19] Y.-R. Chen and **P.-A. Hsiung**, “Automatic Failure Analysis using Safecharts,” *International Journal of Software Engineering and Knowledge Engineering (IJSEKE)*, Vol. 17, No. 1, pp. 57-78, World Scientific Publishing, Singapore, February 2007. (an SEKE’2005 special issue, out of 225 submissions and 115 paper presentations, only 5 papers were published in this special issue) (SCI)
- [20] **P.-A. Hsiung**, Y.-R. Chen, and Y.-H. Lin, “Model Checking Safety-Critical Systems using Safecharts,” *IEEE Transactions on Computers*, Vol. 56, No. 5, pp. 692-705, May 2007. (SCI)
- [21] **P.-A. Hsiung** and S.-W. Lin, “Automatic Synthesis and Verification of Real-Time Embedded Software for Mobile and Ubiquitous Systems,” *Computer Languages, Systems & Structures*, Vol. 34, No. 4, pp. 153–169, Elsevier, The Netherlands, December 2008. (SCI)
- [22] C.-H. Huang and **P.-A. Hsiung**, “Software-Controlled Dynamically Swappable Hardware Design in Partially Reconfigurable Systems,” *EURASIP Journal on Embedded Systems*, Volume 2008, Article ID 231940, 2008. (doi:10.1155/2008/231940) (EI)
- [23] K.-J. Shih, C.-C. Hung, and **P.-A. Hsiung**, “Reconfigurable Hardware Module Sequencer for Dynamically Partially Reconfigurable Systems,” *International Journal of Electrical Engineering (IJEE)*, Vol. 15, No. 2, pp. 87–96, April 2008. (invited for publication in this VLSI Design/CAD Symposium 2007 special issue) (EI)
- [24] **P.-A. Hsiung**, C.-S. Lin, and C.-F. Liao, “Perfecto: A SystemC-based Design Space Exploration Framework for Dynamically Reconfigurable Architectures,” *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, Vol. 1, No. 3, Article 17, September 2008.
- [25] **P.-A. Hsiung**, C.-H. Huang, and Y.-H. Chen, “Hardware Task Scheduling and Placement in Operating Systems for Dynamically Reconfigurable SoC,” *Journal of Embedded Computing (JEC)*, Vol. 3, No. 1, pp. 53–62, IOS Press, The Netherlands, 2009. (an EUC’2005 special issue, out of 376 submissions and 114 paper presentations, only 7 papers were invited for publication in this special issue)
- [26] C. Shih, **P.-A. Hsiung**, T.-K. Liu, Y. Yang, C.-H. Lin, C.-H. Wan, C.-S. Koong, and W. C. Chu, “The Integration of a Vision based Tracking Platform, Visual Instruction and Error Analysis Models for an Efficient Billiard Training System,” *Optical Engineering*, Vol. 48, No. 2, February 2009. (SCI)
- [27] **P.-A. Hsiung**, S.-W. Lin, Y.-R. Chen, C.-H. Huang, and W.C. Chu, “Modeling and Verification of Real-Time Embedded Systems with Urgency,” *Journal of Systems and Software*, Vol. 82, No. 10, pp. 1627–1641, Elsevier Inc., October 2009. (SCI)
- [28] C.-H. Huang and P.-A. Hsiung, “Hardware Resource Virtualization for Dynamically Partially Reconfigurable Systems,” *Embedded Systems Letters*, Volume 1, Issue 1, pp. 19–23, IEEE Press, USA, 2009. (EI)
- [29] C.-S. Lin, **P.-A. Hsiung**, S.-W. Lin, Y.-R. Chen, C.-H. Lu, S.-Y. Tong, W.-T. Su, W. C. Chu, C.-H. Shih, N.-L. Hsueh, C.-H. Chang, and C.-S. Koong, “VERTAF/Multi-Core: A SysML-based Application Framework for Multi-Core Embedded Software Development,” *Journal of the Chinese Institute of Engineers*, Vol. 32, No. 7, pp. 985-991, November 2009 (SCI).

- [30] **P.-A. Hsiung**, S.-W. Lin, and C.-S. Lin, “Real-Time Embedded Software Design for Mobile and Ubiquitous Systems,” *Journal of Signal Processing Systems (JSPS)*, Vol. 59, No. 1, pp. 13, Springer, April 2010 (SCI).
- [31] C.-H. Huang, **P.-A. Hsiung**, and J.-S. Shen, “UML-Based Hardware/Software Co-Design Platform for Dynamically Partially Reconfigurable Network Security Systems,” *Journal of Systems Architecture*, Vol. 56, Nos. 2-3, pp. 88–102, February 2010. (SCI)
- [32] C.-H. Lu, H.-W. Liao, and **P.-A. Hsiung**, “Multi-objective placement of reconfigurable hardware tasks in real-time system,” *International Journal of Embedded Systems*, Vol. 4, No. 3/4, pp. 195–203, Inderscience Publishers, 2010. (EI)
- [33] C.-H. Huang, **P.-A. Hsiung**, and J.-S. Shen, “Model-Based Platform-Specific Co-Design Methodology for Dynamically Partially Reconfigurable Systems with Hardware Virtualization and Preemption,” *Journal of Systems Architecture*, Vol. 56, No. 11, pp. 545–560, November 2010. (SCI)
- [34] **P.-A. Hsiung**, C.-H. Huang, J.-S. Shen, and C.-C. Chiang, “Scheduling and Placement of Hardware/Software Real-Time Relocatable Tasks in Dynamically Partially Reconfigurable Systems,” *ACM Transactions on Reconfigurable Technology and Systems (TRETSS)*, Vol. 4, No. 1, Article 9, December 2010.
- [35] C.-H. Chang, C.-W. Lu, and **P.-A. Hsiung**, “Pattern-based Framework for Modularized Software Development and Evolution Robustness,” *Information and Software Technology (IST)*, Vol. 53, No. 4, pp. 307–316, April 2011. (SCI impact factor: 1.821)
- [36] S.-H. Yang and **P.-A. Hsiung**, “Using RFID in Real-Time Services for Special Education Schools,” *IEEE IT Professional*, Vol. 13, No. 2, pp. 14–19, March/April 2011.
- [37] S.-W. Lin and **P.-A. Hsiung**, “Counterexample-Guided Assume-Guarantee Synthesis Through Learning,” *IEEE Transactions on Computers*, Vol. 60, No. 5, pp. 734–750, May 2011. (SCI)
- [38] C.-S. Lin, C.-H. Lu, S.-W. Lin, Y.-R. Chen, and **P.-A. Hsiung**, “VERTAF/Multi-Core: A SysML-Based Application Framework for Multi-Core Embedded Software Development,” *Journal of Computer Science and Technology*, Vol. 26, No. 3, pp. 448–461, May 2011. (SCI)
- [39] C.-H. Huang and **P.-A. Hsiung**, “Model-based Verification and Estimation Framework for Dynamically Partially Reconfigurable Systems,” *IEEE Transactions on Industrial Informatics*, Vol. 7, No. 2, pp. 287–301, May 2011. (SCI)
- [40] C. Yu, M.-H. Yen, **P.-A. Hsiung**, and S.-J. Chen, “A Low-Power 64-point Pipeline FFT/IFFT Processor for OFDM Applications,” *IEEE Transactions on Consumer Electronics*, Vol. 57, No. 1, pp. 40, February 2011. (SCI)
- [41] N.-L. Hsueh, P.-H. Chu, **P.-A. Hsiung**, M.-J. Chuang, W. Chu, C.-H. Chang, C.-S. Koong, C.-H. Shih, and C.-T. Yang, “A Pattern-based Refactoring Approach for Multi-Core System Design,” *International Journal of Advancements in Computing Technology*, Vol. 3, No. 9, pp. 196–209, AICIT, October 2011 (EI).

- [42] C.S. Koong*, C.H. Shih, **P.A. Hsiung**, H. J. Lai, C. H. Chang, William C. Chu, N. L. Hsueh, C. T. Yang, “Automatic Testing Environment for Multi-core Embedded Software - ATEMES,” *Journal of Systems and Software*, Vol 85, No. 1, pp. 43–60, January 2012. (SCI)
- [43] S.-W. Lin and **P.-A. Hsiung**, “Model Checking Prioritized Timed Systems,” *IEEE Transactions on Computers*, Vol. 61, No. 6, pp. 843–856, June 2012. (SCI)
- [44] W. C.-C. Chu, C.-T. Yang, C.-W. Lu, C.-H. Chang, J.-N. Chen, **P.-A. Hsiung**, H.-M. Lee, “Cloud Computing in Taiwan,” *IEEE Computer*, Vol. 45, No. 6 pp. 42–50, June 2012. (SCI, IF=1.812)
- [45] C. Shih, C.S. Koong, and **P.-A. Hsiung**, “Billiard Combat Modeling and Simulation Based on Optimal Cue Placement Control and Strategic Planning,” *Journal of Intelligent and Robotic Systems*, Vol. 67, No. 1, pp. 25–41, July 2012.
- [46] J.-S. Shen, **P.-A. Hsiung**, and C.-H. Huang, “Learning-based Adaptation to Applications and Environments in a Reconfigurable Network-on-Chip for Reducing Crosstalk and Dynamic Power Consumption,” *Computers & Electrical Engineering*, Elsevier, Vol. 39, No. 2, pp. 453–464, February 2013. (SCI IF=0.837)
- [47] C.-H. Huang and **P.-A. Hsiung**, “Virtualizable Hardware/Software Design Infrastructure for Dynamically Partially Reconfigurable Systems,” *ACM Transactions on Reconfigurable Technology and Systems*, Vol. 6, No. 2, Article 11, July 2013.
- [48] C.-S. Lin, C.-S. Lin, Y.-S. Lin, **P.-A. Hsiung**, and C. Shih, “Multi-Objective Exploitation of Pipeline Parallelism using Clustering, Replication and Duplication in Embedded Multi-core Systems,” *Journal of System Architectures*, Vol. 59, No. 10, Part C, pp. 1083–1094, November 2013.
- [49] H.-L. Chao, C.-C. Wu, C.-Y. Peng, C.-H. Lu, J.-S. Shen, and **P.-A. Hsiung**, “Dynamic Partially Reconfigurable Architecture for Fast Fourier Transform Computation,” *International Journal of Embedded Systems*, Special Issue for EUC’2013, Inderscience Publishers, Vol. 6, Nos. 2-3, pp. 207–215, January 2014. (EI)
- [50] C.-S. Lin, C.-S. Lin, **P.-A. Hsiung**, and W.C. Chu, “Design Issues in a Performance Monitor for Multi-core Embedded Software,” *Journal of Signal Processing Systems*, Vol. 75, No. 2, pp 141–154, May 2014.
- [51] Y.-R. Chen, C.-C. Yeh, **P.-A. Hsiung**, and S.-J. Chen, “Accelerating Coverage Estimation through Partial Model Checking,” *IEEE Transactions on Computers*, Vol. 63, No. 7, pp. 1613–1625, July 2014.
- [52] J.-S. Shen and **P.-A. Hsiung**, “Reasoning and Learning-based Dynamic Codec Reconfiguration for Varying Processing Requirements in Network-on-Chip,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 22, No. 8, pp. 1777–1790, August 2014.
- [53] H.-L. Chao, C.-C. Tsai, **P.-A. Hsiung**, and I.-H. Chou, “Smart Grid as a Service: A Discussion on Design Issues,” *Scientific World Journal*, Hindawi Publishing Corporation, Vol. 2014, Article ID 53508, pp. 1-11, August 2014. (SCI, IF=1.73)

- [54] C.-S. Lin, C.-W. Hsieh, H.-Y. Chang, and **P.-A. Hsiung**, “Efficient Workload Balancing on Heterogeneous GPUs using Mixed Integer Non-Linear Programming,” *Journal of Applied Research and Technology*, Vol. 12, pp. 1176–1186, December 2014. (SCI)
- [55] C.-H. Lu, C.-S. Lin, H.-L. Chao, J.-S. Shen, and **P.-A. Hsiung**, “Reconfigurable Multi-core Architecture – A Plausible Solution to the von Neumann Performance Bottleneck,” *International Journal of Adaptive and Innovative Systems*, Special Issue for MCSoc’2013, Inderscience Publishers, Vol. 2, No. 3, pp. 217–231, 2015.
- [56] C.-S. Lin, S.-M. Teng, and **P.-A. Hsiung**, “Auto-tuning for GPGPU applications using Performance and Energy Model,” *Journal of Systems Architecture*, Vol. 62, pp. 40–53, January 2016.
- [57] C.-H. Chang, C.-W. Lu, W. C.-C. Chu, and **P.-A. Hsiung**, “SysML-based Requirement Management to Improve Software Development,” *International Journal of Software Engineering and Knowledge Engineering*, Vol. 26, No. 3, pp. 491–511, April 2016. (SCI)
- [58] H.-L. Chao and **P.-A. Hsiung**, “A Fair Energy Resource Allocation Strategy for Micro Grid,” *Microprocessors and Microsystems*, Vol. 42, pp. 235–244, May 2016.
- [59] H.-L. Chao, S.-Y. Tong, and **P.-A. Hsiung**, “Dynamic Task Mapping with Congestion Speculation for Reconfigurable Network-on-Chip,” *ACM Transactions on Reconfigurable Technology and Systems (TRETs)*, Vol. 10, No. 1, Article 3, September 2016.
- [60] C.-H. Huang, C.-Y. Wang, and **P.-A. Hsiung**, “Elastic Superposition Task Mapping for NoC-based Reconfigurable Systems,” *Microprocessors and Microsystems*, Vol. 51, pp. 297–312, June 2017.

(B) Books and Chapters

- [61] **P.-A. Hsiung**, *System Level Synthesis for Parallel Computers*, Ph.D. Dissertation, Graduate Institute of Electrical Engineering, National Taiwan University, June 1996.
- [62] H. Arabnia, Editor, **P.-A. Hsiung**, et al. Associate Editor, *Proceedings of the 1999 International Conference on Parallel and Distributed Processing Techniques and Applications*, Volumes I-VI, Computer Science Research, Education, and Applications (CSREA) Press (ISBN), USA, June 1999.
- [63] **P.-A. Hsiung** and Farn Wang (Editors), *Proceedings of the International Workshop on Real-Time Constraints*, (RTC’99, Alexandria, Virginia, USA), October 1999.
- [64] **P.-A. Hsiung** (Program Chair), *Proceedings of the International Workshop on Distributed System Validation and Verification*, (DSVV’2000, Taipei, Taiwan, ROC), April 2000.
- [65] **P.-A. Hsiung**, “Real-Time Constraints,” in *Encyclopedia of Computer Science and Technology*, Allen Kent and James G. Williams, Editors, Volume 45 - Supplement 30, (ISBN: 0-8247-2298-1), pp. 285–309, Marcel Dekker, Inc., New York, USA, 2002.
- [66] **P.-A. Hsiung**, Y.-H. Lin, Y.-R. Chen, “Safecharts Model Checking for the Verification of Safety-Critical Systems,” in *Verification, Validation and Testing in Software Engineering*, editors Aristides Dasso, Ana Funes, IDEA Group, Inc., USA, 2007.

- [67] K.-J. Shih and **P.-A. Hsiung**, “Reconfigurable Computing Technologies Overview,” *Encyclopedia of Information Science and Technology*, 2nd ed., IGI Global, USA, 2007.
- [68] **P.-A. Hsiung**, M. D. Santambrogio, and C.-H. Huang, *Reconfigurable System Design and Verification*, CRC Press, USA, February 2009.
- [69] J.-S. Shen and **P.-A. Hsiung**, *Dynamic Reconfigurable Network-on-Chip Design: Innovations for Computational Processing and Communication*, IGI Global, USA, 2009.
- [70] S.-J. Chen, G.-H. Lin, **P.-A. Hsiung**, and Y.-H. Hu, *Hardware-Software Co-design of a Multimedia SoC Platform*, Springer, USA, 2009.
- [71] W.-W. Lin, J.-S. Shen, and **P.-A. Hsiung**, “An Efficient Hardware-Software Communication Mechanism for Reconfigurable Network-on-Chip,” *Dynamic Reconfigurable Network-on-Chip Design: Innovations for Computational Processing and Communication*, IGI Global, USA, 2010.
- [72] S.-W. Lin, C.-S. Lin, C.-H. Lu, Y.-R. Chen, and **P.-A. Hsiung**, “Model-Driven Development of Multi-Core Embedded Software,” *Modern Software Engineering Concepts and Practices: Advanced Approaches*, Editors: Ali H. Dogru and Veli Bicer, Chapter 15, pp. 357-379, IGI Global, USA, December 2010.
- [73] C.-H. Lin, K.-S. Hwang, **P.-A. Hsiung**, M.-H. Yen, Y. Chu, S.-J. Chen, W. C. Chu, “An Adaptive Reasoning and Learning Framework for Mobile Cognitive Radio Systems,” *Handbook of Research on Mobile Software Engineering*, Editors: Paulo Alencar and Donald Cowan, Chapter 21, pp. 361–378, IGI Global, USA, May 2012.
- [74] **P.-A. Hsiung** and S.-W. Lin, “Automatic Synthesis and Verification of Real-Time Embedded Software for Mobile and Ubiquitous Systems,” in *Handbook on Mobile and Ubiquitous Computing Innovations: Status and Perspectives*, Editors: Laurence T. Yang, Evi Syukur, and Seng W. Loke, Chapter 16, pp. 395–416, CRC Press, USA, October 2012.

(C) International Conference Papers

- [75] **P.-A. Hsiung**, T.-Y. Lee, and S.-J. Chen, “Object-Oriented Technology Transfer to Multi-processor System-Level Synthesis,” In *Proc. of the 24th International Conference on Technology of Object-Oriented Languages and Systems (TOOLS’97)*, pp. 339–348, September 1997.
- [76] F. Wang and **P.-A. Hsiung**, “Parametric Analysis of Computer Systems,” In *Proc. of the 6th International AMAST Conference*, Lecture Notes in Computer Science (LNCS), pp. 539–553, Springer-Verlag, Vol. 1349, December 1997.
- [77] **P.-A. Hsiung**, T.-Y. Lee, and S.-J. Chen, “CMAPS: A Cosynthesis Methodology for Application-Oriented General-Purpose Parallel Systems,” In *Proc. of the 2nd IMACS-IEEE International Multiconference on Computational Engineering in Systems Applications (CESA’98)*, Special Session on System Level Hardware/Software Codesign, Vol. 1, pp. 1222–1227, Tunisia, April 1998.
- [78] **P.-A. Hsiung**, “Parallel Design Automation of Computer Systems,” In *Proc. International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA’98)*, Vol. 1, pp. 183-190, Las Vegas, Nevada, USA, July 1998.

- [79] **P.-A. Hsiung**, “Object-Oriented Application Framework Design for Real-Time Systems,” *In Proc. 4th International Symposium on Real-Time and Media Systems*, (RAMS’98), pp. 221–227, Taipei, Taiwan, September 1998.
- [80] **P.-A. Hsiung**, “Parallel Object-Oriented Synthesis Environment Based on Message-Passing,” *In Proc. 27th International Conference on Technology of Object-Oriented Languages and Systems*, (TOOLS’98), Beijing, China, pp. 251–255, September 1998.
- [81] **P.-A. Hsiung**, “RTFrame: An Object-Oriented Application Framework for Real-Time Applications,” *In Proc. 27th International Conference on Technology of Object-Oriented Languages and Systems*, (TOOLS’98), Beijing, China, pp. 138–147, September 1998.
- [82] **P.-A. Hsiung** and F. Wang, “A State Graph Manipulator Tool for Real-Time System Specification and Verification,” *In Proc. 4th International Conference on Real-Time Computing Systems and Applications*, (RTCSA’98), pp. 181–188, Hiroshima, Japan, October 1998.
- [83] F. Wang and **P.-A. Hsiung**, “Verification on the Large,” *In Proc. 3rd IEEE High-Assurance Systems Engineering Symposium*, (HASE’98), pp. 134–141, Washington D.C., USA, November 1998 (**invited paper**).
- [84] **P.-A. Hsiung**, “MISSE: A Multi-level Intelligent Synthesis and Simulation Environment,” *In Proc. of the International Computer Symposium (ICS’98)*, Workshop on Computer Architecture, pp. 52–59, Tainan, Taiwan, December 1998.
- [85] **P.-A. Hsiung**, F. Wang, and Y. S. Kuo, “Scheduling System Verification,” *In Proc. of the 5th International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS’99)*, Lecture Notes in Computer Science (LNCS), Vol. 1579, pp. 19–33, Springer-Verlag, Amsterdam, the Netherlands, March 1999.
- [86] **P.-A. Hsiung**, “Timing Coverification of Concurrent Embedded Real-Time Systems,” *In Proc. of the 7th International Workshop on Hardware-Software Codesign (CODES’99)*, Rome, Italy, pp. 110–114, ACM Press, New York, USA, May 1999.
- [87] **P.-A. Hsiung**, “Hardware-Software Coverification of Concurrent Embedded Real-Time Systems,” *In Proc. of the 11th Euromicro Conference on Real-Time Systems (ECRTS’99)*, York, England, pp. 216–223, IEEE CS Press, June 1999.
- [88] T.-Y. Lee, **P.-A. Hsiung**, and S.-J. Chen, “A Case Study in Hardware-Software Codesign of Distributed Systems — Vehicle Parking Management System,” *In Proc. of the 1999 International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA’99)*, Las Vegas, Vol. VI, pp. 2982–2987, CSREA Press, USA, June 1999.
- [89] **P.-A. Hsiung**, “High Level Design Reuse Through Fuzzy Learning,” *In Proc. of the International Conference on Artificial Intelligence (IC-AI’99)*, Las Vegas, Vol. II, pp. 658–661, CSREA Press, USA, July 1999.
- [90] **P.-A. Hsiung**, “Parallel Object-Oriented Synthesis Methodology,” *In Proc. of the 1999 International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA’99)*, Las Vegas, Vol. IV, pp. 2073–2076, CSREA Press, USA, June 1999.

- [91] **P.-A. Hsiung** and F. Wang, “User Friendly Verification,” In *Proc. of the 1999 IFIP TC6/WG6.1 Joint International Conference on Formal Description Techniques For Distributed Systems and Communication Protocols & Protocol Specification, Testing, And Verification*, (FORTE/PSTV ’99, Beijing, China), October 1999.
- [92] **P.-A. Hsiung** and F. Wang, “State Graph Manipulators,” In *Proc. of the International Workshop on Real-Time Constraints*, (RTC’99, Alexandria, Virginia, USA), pp. 40-52, October 1999.
- [93] **P.-A. Hsiung**, F. Wang, and Y.-S. Kuo, “Verification of Concurrent Client-Server Real-Time Scheduling Systems,” In *Proc. of the 6th International Conference on Real-Time Computing Systems and Applications*, (RTCSA’99, Hong-Kong, China), pp. 228–235, December 1999.
- [94] J.-M. Fu, W.-B. See, **P.-A. Hsiung**, J.-M. Chao, and S.-J. Chen, “A Java-Based Distributed System Framework for Real-Time Development,” In *Proc. of the International Workshop on Distributed Real-Time Systems* (IWDRS’2000, Taipei, Taiwan, ROC), pp. B-31 – B-36, IEEE CS Press, USA, April 2000.
- [95] **P.-A. Hsiung**, “Concurrent Embedded Real-Time Software Verification,” In *Proc. the 24th IEEE Computer Society International Computer Software and Applications Conference* (COMP-SAC’00, Taipei, Taiwan, ROC), pp. 516–521, IEEE Computer Society Press, USA, October 2000.
- [96] **P.-A. Hsiung**, “Synthesis of Parametric Embedded Real-Time Software,” In *Proc. of the International Computer Symposium*, (ICS’2000, Taiwan), Workshop on Computer Architecture, pp. 144–151, ISBN 957-02-7308-9, December 2000.
- [97] **P.-A. Hsiung**, F. Wang, R.-C. Chen, “On the Verification of Wireless Transaction Protocol Using SGM and RED,” In *Proc. the 7th IEEE International Conference on Real-Time Computing Systems and Applications* (RTCSA’00, Korea), pp. 379–383, IEEE Computer Society Press, USA, December 2000.
- [98] **P.-A. Hsiung**, “Formal Synthesis and Code Generation of Embedded Real-Time Software,” In *Proc. of the ACM/IEEE 9th International Symposium on Hardware/Software Codesign* (CODES’01, Copenhagen, Denmark), pp. 208–213, ACM Press, New York, USA, April 2001.
- [99] **P.-A. Hsiung**, F.-S. Su, C.-H. Gao, and Y.-M. Chang, “Verifiable Embedded Real-Time Application Framework,” In *Proc. of the IEEE International Real-Time Technology and Applications Symposium* (RTAS’01), Work-In-Progress Session, (Taipei, Taiwan), pp. 109–110, IEEE Computer Society Press, May 2001.
- [100] **P.-A. Hsiung**, “Formal Synthesis and Control of Soft Embedded Real-Time Systems,” In *Proc. of the 21st International Conference on Formal Techniques for Networked and Distributed Systems* (FORTE’01, Cheju Island, Korea), pp. 35–50, Kluwer Academic Publishers, August 2001.
- [101] **P.-A. Hsiung**, W.-B. See, T.-Y. Lee, J.-M. Fu, and S.-J. Chen, “Formal Verification of Embedded Real-Time Software in Component-Based Application Frameworks,” In *Proc. of the 8th Asia-Pacific Software Engineering Conference* (APSEC’01, Macau SAR, China),

pp. 71–78, IEEE CS Press, December 2001 (acceptance rate for regular papers: 44/145 = 30%).

- [102] C.-H. Gau and **P.-A. Hsiung**, “Time-Memory Scheduling and Code Generation of Real-Time Embedded Software,” In *Proc. of the 8th International Conference on Real-Time Computing Systems and Applications (RTCSA’02, Tokyo, Japan)*, pp. 19–27, March 2002.
- [103] **P.-A. Hsiung** and C.-H. Gau, “Formal Synthesis of Real-Time Embedded Software by Time-Memory Scheduling of Colored Time Petri Nets,” In *Proc. of the Workshop on Theory and Practice of Timed Systems (TPTS’2002, Grenoble, France)*, Electronic Notes in Theoretical Computer Science (ENTCS), April 2002.
- [104] **P.-A. Hsiung**, T.-Y. Lee, W.-B. See, J.-M. Fu, and S.-J. Chen, “VERTAF: An Object-Oriented Application Framework for Embedded Real-Time Systems,” In *Proc. of the 5th IEEE International Symposium on Object-Oriented Real-Time Distributed Computing (ISORC’02, Washington, D.C., USA)*, pp. 322–329, IEEE CS Press, April 2002.
- [105] F.-S. Su and **P.-A. Hsiung**, “Extended Quasi-Static Scheduling for Formal Synthesis and Code Generation of Embedded Software,” In *Proc. of the 10th IEEE/ACM International Symposium on Hardware/Software Codesign (CODES’02, Colorado, USA)*, IEEE CS Press, pp. 211–216, May 2002.
- [106] **P.-A. Hsiung**, T.-Y. Lee, and F.-S. Su, “Formal Synthesis and Code Generation of Real-Time Embedded Software using Time-Extended Quasi-Static Scheduling,” In *Proc. of the 9th Asia-Pacific Software Engineering Conference (APSEC’2002, Queensland, Australia)*, pp. 395–404, IEEE CS Press, December 2002.
- [107] T.-Y. Lee, **P.-A. Hsiung**, and S.-J. Chen, “TCN: Scalable Hierarchical Hypercubes,” In *Proc. of the 2002 International Conference on Parallel and Distributed Systems (ICPADS’2002, NCU, Taiwan)*, pp. 11–16, December 2002.
- [108] **P.-A. Hsiung** and S.-Y. Cheng, “Automating Formal Modular Verification of Asynchronous Real-Time Embedded Systems,” In *Proc. of the International Computer Symposium, (ICS’2002, NDHU, Taiwan)*, pp. 173-179, December 2002.
- [109] T.-Y. Lee, **P.-A. Hsiung**, I-Mu Wu, and Feng-Shi Su, “ESSP: An Embedded Software Synthesis and Prototyping Methodology,” In *Proc. of the International Computer Symposium, (ICS’2002, NDHU, Taiwan)*, pp. 150–157, December 2002.
- [110] **P.-A. Hsiung** and S.-Y. Cheng, “Automating Formal Modular Verification of Asynchronous Real-Time Embedded Systems,” In *Proc. of the 16th International Conference on VLSI Design, (VLSI’2003, New Delhi, India)*, pp. 249–254, January 2003.
- [111] **P.-A. Hsiung** and F.-S. Su, “Synthesis of Real-Time Embedded Software by Timed Quasi-Static Scheduling,” In *Proc. of the 16th International Conference on VLSI Design, (VLSI’2003, New Delhi, India)*, pp. 579–584, January 2003.
- [112] **P.-A. Hsiung**, C.-Y. Lin, and T.-Y. Lee, “Quasi-Dynamic Scheduling for the Synthesis of Real-Time Embedded Software with Local and Global Deadlines,” In *Proc. of the 9th International Conference on Real-Time and Embedded Computing Systems and Applications (RTCSA’2003, Tainan, Taiwan)*, February 2003.

- [113] T.-Y. Lee, **P.-A. Hsiung**, I.-M. Wu, and F.-S. Su, “RESS: Real-Time Embedded Software Synthesis and Prototyping Methodology,” In *Proc. of the 9th International Conference on Real-Time and Embedded Computing Systems and Applications (RTCSA’2003, Tainan, Taiwan)*, February 2003.
- [114] W.-B. See, **P.-A. Hsiung**, S.-J. Chen, “Software Platform for Embedded Software Development,” In *Proc. of the 9th International Conference on Real-Time and Embedded Computing Systems and Applications (RTCSA’2003, Tainan, Taiwan)*, February 2003.
- [115] W.-S. Liao and **P.-A. Hsiung**, “FVP: A Formal Verification Platform for SoC,” In *Proc. of the 16th IEEE International SoC Conference*, Portland, Oregon, USA, pp. 21–24, September 2003.
- [116] W.-B. See, **P.-A. Hsiung**, and S.-J. Chen, “Framework Approach for System on Chip Software Development,” In *Proc. of the International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA, Hsinchu, Taiwan)*, pp. 196–199, October 2003.
- [117] W.-B. See, **P.-A. Hsiung**, and S.-J. Chen, “An Affordable Dispatching System for Logistic Applications,” In *Proc. of the 6th Asia-Pacific Intelligent Transportation Systems Forum*, Taipei, Taiwan, pp. 283, October 2003.
- [118] **P.-A. Hsiung** and C.-Y. Lin, “Synthesis of Real-Time Embedded Software with Local and Global Deadlines,” In *Proc. of the IEEE/ACM International Symposium on Hardware-Software Codesign and System Synthesis (CODES-ISSS 2003)*, ACM Press, California, USA, pp. 114–119, October 2003 (acceptance rate = $30/143 = 21\%$).
- [119] T.-Y. Lee, **P.-A. Hsiung**, I.-M. Wu, C.-C. Tsai, and W.-T. Lee, “The Design of a Synthesis Tool for Interrupt-based Real-Time Embedded Software,” In *Proc. of the 2003 International Conference on Informatics, Cybernetics, and Systems (ICICS 2003)*, pp. 1284–1289, December 2003.
- [120] W.-S. Liao and **P.-A. Hsiung**, “Creating a Formal Verification Platform for IBM CoreConnect-based SoC,” In *Proc. of the 1st International Workshop on Automated Technology for Verification and Analysis (ATVA 2003)*, pp. 7–18, December 2003.
- [121] **P.-A. Hsiung** and S.-W. Lin, “Automatic Synthesis and Verification of Real-Time Embedded Software,” In *Proc. of the International Conference on Embedded and Ubiquitous Computing*, LNCS, Vol. 3207, pp. 12-21, Springer Verlag, (EUC’2004, Aizu-Wakamatsu, Japan), August 2004 (**Best Paper Candidate**).
- [122] T.-C. Lee and **P.-A. Hsiung**, “Mutation Coverage Estimation for Model Checking,” In *Proc. of the 2nd International Symposium on Automated Technology for Verification and Analysis (ATVA, Taipei, Taiwan)*, LNCS Vol. 3299, pp. 354–368, Springer Verlag, October 2004.
- [123] **P.-A. Hsiung** and S.-W. Lin, “Formal Design and Verification of Real-Time Embedded Software,” In *Proc. of the 2nd Asian Symposium on Programming Languages and Systems (APLAS, Taipei, Taiwan)*, LNCS Vol. 3302, pp. 382–397, Springer Verlag, November 2004 (acceptance rate = $26/97 = 26.8\%$).
- [124] **P.-A. Hsiung** and H.-C. Kao, “Device-Centric Low-Power Scheduling for Real-Time Embedded Systems,” In *Proc. of the International Embedded and Hybrid Systems Conference (IEHSC, Singapore)*, Vol. 15, No. 2, pp. 461–466, April 2005.

- [125] **P.-A. Hsiung** and Y.-H. Lin, “Model-based Verification of Safety-Critical Systems,” In *Proc. of the 17th International Conference on Software Engineering and Knowledge Engineering (SEKE, Taiwan, ROC)*, pp. 596–601, Knowledge Systems Institute Graduate School, July 2005.
- [126] **P.-A. Hsiung** and S.-W. Lin, “Model Checking Timed Systems with Priorities,” In *Proceedings of the International Conference on Real-Time and Embedded Computing Systems and Applications (RTCSA, Hong-Kong, China)*, pp. 539–544, IEEE CS Press, August 2005.
- [127] S.-W. Lin, **P.-A. Hsiung**, C.-H. Huang, and Y.-R. Chen, “Model Checking Prioritized Timed Automata,” In *Proceedings of the 3rd International Symposium on Automated Technology for Verification and Analysis (ATVA, Taipei, Taiwan)*, LNCS Vol. 3707, pp. 370–384, Springer Verlag, October 2005.
- [128] **P.-A. Hsiung** and Y.-H. Lin, “Modeling and Verification of Safety-Critical Systems using Safecharts,” In *Proceedings of the 25th IFIP WG 6.1 International Conference on Formal Techniques for Networked and Distributed Systems (FORTE, Taipei, Taiwan)*, LNCS Vol. 3731, pp. 290–304, Springer Verlag, October 2005.
- [129] C.-H. Tseng and **P.-A. Hsiung**, “UML-Based Design Flow and Partitioning Methodology for Dynamically Reconfigurable Computing Systems,” In *Proceedings of the 2005 IFIP International Conference on Embedded and Ubiquitous Computing (EUC’2005, Nagasaki, Japan)*, Lecture Notes in Computer Science (LNCS), Vol. 3824, pp. 479–488, December 2005.
- [130] Y.-H. Chen and **P.-A. Hsiung**, “Hardware Task Scheduling and Placement in Operating Systems for Dynamically Reconfigurable SoC,” In *Proceedings of the 2005 IFIP International Conference on Embedded and Ubiquitous Computing (EUC’2005, Nagasaki, Japan)*, Lecture Notes in Computer Science (LNCS), Vol. 3824, pp. 489–498, Springer Verlag, December 2005.
- [131] C.-H. Tseng and **P.-A. Hsiung**, “A UML-Based Design Flow and Partitioning Methodology for Dynamically Reconfigurable Systems,” In *Proceedings of the 3rd International DAC Workshop, UML for SoC Design (UML-SoC’2006, San Francisco, CA, USA)*, July 2006.
- [132] **P.-A. Hsiung**, C.-H. Huang, and C.-F. Liao, “Perfecto: A SystemC-based Performance Evaluation Framework for Dynamically Partially Reconfigurable Systems,” In *Proceedings of the 16th International Conference on Field Programmable Logic and Applications (FPL’2006, Madrid, Spain)*, pp. 190–198, IEEE CS Press, August 2006.
- [133] **P.-A. Hsiung**, S.-W. Lin, Y.-R. Chen, C.-H. Huang, J.-J. Yeh, H.-Y. Sun, C.-S. Lin, and H.-W. Liao, “Model Checking Timed Systems with Urgencies,” *Proceedings of the 4th International Symposium on Automated Technology for Verification and Analysis (ATVA, Beijing, China)*, LNCS Vol. 4218, pp. 67–81, Springer-Verlag, October 2006. (Acceptance Rate = $35/137 = 25.6\%$)
- [134] J.-Y. Chien, C.-Y. Wu, K.-H. Lin, **P.-A. Hsiung**, “RFID-based Automatic Airport Baggage Handling System,” *Proceedings of the International Computer Symposium, (ICS)*, pp. 62–67, December 2006.

- [135] C.-H. Huang, K.-J. Shih, C.-S. Lin, S.-S. Chang, and **P.-A. Hsiung**, “Dynamically Swappable Hardware Design in Partially Reconfigurable Systems,” *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS, New Orleans, USA)*, pp. 2742-2745, IEEE Press, May 2007.
- [136] Y.-R. Chen, **P.-A. Hsiung**, S.-J. Chen, “Modeling and Automatic Failure Analysis of Safety-Critical Systems using Extended Safecharts,” *Proceedings of the International Conference on Computer Safety, Reliability and Security (SAFECOMP), Nuremberg, Germany, Lecture Notes in Computer Science (LNCS), Vol. 4680*, pp. 451–464, Springer Verlag, September 2007. (Acceptance Rate = $33/136 = 24.26\%$)
- [137] **P.-A. Hsiung** and C.-W. Liu, “Exploiting Hardware and Software Low Power Techniques for Energy Efficient Co-scheduling in Dynamically Reconfigurable Systems,” *Proceedings of the 17th International Conference on Field Programmable Logic and Applications, (FPL, Amsterdam, Netherlands)*, pp. 165–170, IEEE CS Press, August 2007. (Acceptance Rate: $67/302 = 23\%$)
- [138] **P.-A. Hsiung**, P.-H. Lu, and C.-W. Liu, “Energy Efficient Hardware-Software Co-scheduling in Dynamically Reconfigurable Systems,” *Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis, (CODES+ISSS, Salzburg, Austria)*, pp. 87–92, ACM Press, September 2007. (Acceptance Rate: $40/127 = 31\%$).
- [139] K.-J. Shih, C.-C. Hung, and **P.-A. Hsiung**, “Reconfigurable Hardware Module Sequencer – A Tradeoff Between Networked and Data Flow Architectures,” *Proceedings of the IEEE International Conference on Field-Programmable Technology (ICFPT’07, Japan)*, pp. 237–240, December 2007.
- [140] **P.-A. Hsiung** and S.-W. Lin, “From ISA to Application Design via RTOS – A Course Design Framework for Embedded Software,” *Proceedings of the 1st Asia-Pacific Workshop on Embedded System Education and Research (APESER’07, Hsinchu, Taiwan)*, December 2007.
- [141] **P.-A. Hsiung**, S.-W. Lin, C.-C. Hung, J.-M. Fu, C.-S. Lin, C.-C. Chiang, K.-C. Chiang, C.-H. Lu, and P.-H. Lu “Real-Time Embedded Software Design for Mobile and Ubiquitous Systems,” *Proceedings of the IFIP International Conference on Embedded and Ubiquitous Computing (EUC’07, Taipei, Taiwan)*, Lecture Notes in Computer Science (LNCS) Vol. 4808, pp. 718–729, Springer Verlag, December 2007.
- [142] C.-H. Huang and **P.-A. Hsiung**, “UML-Based Hardware/Software Co-Design for Partially Reconfigurable Systems,” *Proceedings of the 13th IEEE Asia-Pacific Computer Systems Architecture Conference (ACSAC)*, August 2008.
- [143] J.-S. Sheng, **P.-A. Hsiung**, and K.-C. Chang, “A Novel Spatio-Temporal Adaptive Bus Encoding for Reducing Crosstalk Interferences with Trade-Offs Between Performance and Reliability,” *Proceedings of the 13th IEEE Asia-Pacific Computer Systems Architecture Conference (ACSAC)*, August 2008.
- [144] Y. Chu, M.-H. Yen, **P.-A. Hsiung**, and S.-J. Chen, “Design of a High-Speed Block Interleaving/Deinterleaving Architecture for Wireless Communication Applications,” *Proceedings of the 27th IEEE International Conference on Consumer Electronics (ICCE)*, January 2009.

- [145] C.-H. Huang and **P.-A. Hsiung**, “On the Use of a UML-Based HW/SW Co-Design Platform for Reconfigurable Cryptographic Systems,” *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, Taipei, Taiwan, May 2009.
- [146] J.W. Lin, D.-T. Yen, W.-Y. Hu, C. Yu, M.-H. Yen, **P.-A. Hsiung**, and S.-J. Chen, “A 900 MHz to 5.2 GHz Dual-Loop Feedback Multi-band LNA,” *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, Taipei, Taiwan, May 2009.
- [147] **P.-A. Hsiung**, S.-W. Lin, Y.-R. Chen, N.-L. Hsueh, C.-H. Chang, C.-H. Shih, C.-S. Koong, C.-S. Lin, C.-H. Lu, S.-Y. Tong, W.-T. Sun, and W. C. Chu, “Model-Driven Development of Multi-Core Embedded Software,” *Proceedings of the 2nd International Workshop on Multi-core Software Engineering (IWMSE)*, May 2009.
- [148] **P.-A. Hsiung**, C.-S. Lin, S.-W. Lin, Y.-R. Chen, C.-H. Lu, S.-Y. Tong, W.-T. Su, C. Shih, C.-S. Koong, N.-L. Hsueh, C.-H. Chang, and W. C. Chu, “VERTAF/Multi-Core: A SysML-based Application Framework for Multi-Core Embedded Software Development,” *Proceedings of the 9th International Conference on Algorithms and Architectures for Parallel Processing (ICA3PP)*, Taipei, Taiwan, June 2009.
- [149] Y.-R. Chen, T.-Y. Chen, **P.-A. Hsiung**, S.-J. Chen, and Y.-H. Hu, “Compositional Automata Reduction with Non-critical Path Slicing,” *Proceedings of the International Conference on Foundations of Computer Science (FCS, Las Vegas, Nevada, USA)*, July 2009.
- [150] J. C. Lin, C. Yu, M. S. Yen, **P. A. Hsiung**, S. J. Chen, and Y. H. Hu, “Parallel Implementation of Convolution Encoder for Software Defined Radio on DSP Architecture,” *Proceedings of the International Symposium on Systems, Architectures, Modeling, and Simulation (SAMOS)*, Greece, pp. 180–186, July 2009.
- [151] C. Shih, **P.-A. Hsiung**, N.-L. Hsueh, C.-H. Chang, C.-S. Koong, and W. C. Chu, “A Model-Driven Multicore Software Development Environment for Embedded System,” *Proceedings of the 3rd IEEE International Workshop on Quality Oriented Reuse of Software (QUORS)*, Seattle, Washington, USA, July 2009.
- [152] C. Shih, C.-T. Wu, C.-Y. Lin, **P.-A. Hsiung**, N.-L. Hsueh, C.-H. Chang, C.-S. Koong, and W. C. Chu, “A Model-Driven Multicore Software Development Environment for Embedded System,” *Proceedings of the 33rd IEEE International Computer Software and Applications Conference*, Washington, USA, IEEE CS Press, July 2009.
- [153] C.-H. Lu, Hsiao-Win Liao, and **P.-A. Hsiung**, “Multi-Objective Placement of Reconfigurable Hardware Tasks in Real-Time System,” *Proceedings of the International Workshop on Reconfigurable and Multicore Embedded Systems*, (WoRMES, Vancouver, Canada), IEEE CS Press, August 2009.
- [154] K.-J. Shih, Y.-H. Lin, and **P.-A. Hsiung**, “Quality-of-Service Optimization for Multiple Multimedia Tasks in Real-Time Embedded Systems,” *Proceedings of the 10th International Symposium on Pervasive Systems, Algorithms and Networks (I-SPAN)*, Kaohsiung, Taiwan, December 2009.
- [155] C.-H. Lu, K.-C. Chiang, and **P.-A. Hsiung**, “Round-based Priority Arbitration for Predictable and Reconfigurable Network-on-Chip,” *Proceedings of the International Conference on Field-Programmable Technology (FPT)*, Sydney, Australia, December 2009.

- [156] J.-S. Shen, C.-H. Huang, and **P.-A. Hsiung**, “PRESSNoC: Power-Aware and Reliable Encoding Schemes Supported Reconfigurable Network-on-Chip Architecture,” *Proceedings of the Fourth International Conference on Embedded and Multimedia Computing*, (EM-Com), Jeju, Korea, December 2009. (*Best Paper Award*)
- [157] S.-H. Yang and **P.-A. Hsiung**, “RFID Campus for Special Education Schools,” *Proceedings of the Asian Pacific International Conference on RFID*, Taipei, Taiwan, December 2009.
- [158] J.-S. Shen, C.-H. Huang, and **P.-A. Hsiung**, “Learning-based Adaptation to Applications and Environments in a Reconfigurable Network-on-Chip,” *Proceedings of the Design, Automation & Test in Europe* (DATE), Dresden, Germany, March 2010.
- [159] C.-H. Chang, C.-W. Lu, W. C. Chu, C.-H. Shih, C.-T. Yang, **P.-A. Hsiung**, N.-L. Hsueh, and C.-S. Koong, “SysML-based Requirement Modeling Environment for Multicore Embedded System,” *Proceedings of the 25th ACM Symposium on Applied Computing* (SAC, Sierre, Switzerland), ACM Press, March 2010.
- [160] C.-J. Chen, C. Yu, M.-H. Yen, **P.-A. Hsiung**, and S.-J. Chen, “Design of a Low Power Viterbi Decoder for Wireless Communication Applications,” *Proceedings of the 14th IEEE International Symposium on Consumer Electronics* (ISCE, Braunschweig, Germany), June 2010.
- [161] N.-L. Hsueh, P.-H. Chu, **P.-A. Hsiung**, M.-J. Chuang, W. Chu, C.-H. Chang, C.-S. Koong, C.-H. Shih “Supporting Design Enhancement by Pattern-based Transformation,” *Proceedings of the IEEE Computer Software and Applications Conference* (COMPSAC), 2010.
- [162] S.-H. Yang and **P.-A. Hsiung**, “Innovative Application of RFID Systems to Special Education Schools,” *Proceedings of the 5th IEEE International Conference on Networking, Architecture, and Storage* (NAS), Macau SAR, China, July 2010
- [163] Y.-R. Chen, W.-T. Su, **P.-A. Hsiung**, Y.-C. Lan, Y.-H. Hu, and S.-J. Chen, “Formal Modeling and Verification of Network-on-Chip,” *Proceedings of the International Conference on Green Circuits and Systems*, (ICGCS), 2010.
- [164] S. J. Chen, **P. A. Hsiung**, C. Yu, M.-H. Yen, S. Sezer, M. Schulte, and Y. H. Hu, “ARAL-CR: An Adaptive Reasoning And Learning Cognitive Radio Platform,” *International Symposium on Systems: Architectures, Modeling, and Simulation* (SAMOS), Greece, July 2010.
- [165] K.-J. Shih, H.-Y. Sun, and **P.-A. Hsiung**, “Dynamic Hardware-Software Task Switching and Relocation Mechanisms for Reconfigurable Systems,” *Proceedings of the IET International Conference on Frontier Computing – Theory, Technologies and Applications*, Taichung, Taiwan, August 2010.
- [166] S.-S. Lu, C.-H. Lu, and **P.-A. Hsiung**, “Congestion- and Energy-aware Run-Time Mapping for Tile-Based Network-On-Chip Architecture,” *Proceedings of the IET International Conference on Frontier Computing – Theory, Technologies and Applications*, Taichung, Taiwan, August 2010.
- [167] K.-S. Huang, C.-H. Lin, and **P.-A. Hsiung**, *A Space-Efficient and Multi-Objective Case-Based Reasoning in Cognitive Radio*,” *Proceedings of the IET International Conference on Frontier Computing – Theory, Technologies and Applications*, Taichung, Taiwan, August 2010.

- [168] C.-H. Huang, J.-S. Shen, and **P.-A. Hsiung**, “A Self-Adaptive Hardware/Software System Architecture for Ubiquitous Computing Applications,” *Proceedings of the 7th International Conference on Ubiquitous Intelligence and Computing*, (UIC 2010, Xi’an, China), LNCS Vol. 6406, pp. 382–396, Springer Verlag, October 2010.
- [169] J.-S. Shen, W.-T. Su, and P.-A. Hsiung, “Network-on-Chip Router Design with Buffer-Stealing,” *Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC, Yokohama, Japan)*, January 2011 (accepted for presentation).
- [170] Y. Chu, Y.-T. Liao, M.-H. Yen, **P.-A. Hsiung**, and S.-J. Chen, “A Novel Low-Power 64-Point Pipelined FFT/IFFT Processor for OFDM Applications,” *Proceedings of the IEEE International Conference on Consumer Electronics (ICCE, Las Vegas, USA)*, January 2011 (accepted for presentation).
- [171] P.-H. Chu, N.-L. Hsueh, C.-C. Lee, M.-J. Chuang, **P.-A. Hsiung**, and W. Chu, “A Pattern-based Verification Approach for a Multi-Core System Development,” *Proceedings of the 26th ACM Symposium on Applied Computing (SAC, Taichung, Taiwan)*, ACM Press, March 2011.
- [172] C.-H. Chang, C.-W. Lu, W.C. Chu, C.-T. Yang, **P.-A. Hsiung**, N.-L. Hsueh, and C.-S. Koong, “XML-based Reusable Component Repository for Embedded Software,” *Proceedings of the 5th IEEE International Workshop on Quality Oriented Reuse of Software*, (QUORS, Munich, Germany), July 2011.
- [173] C.H. Chang; C.W. Lu; C.W. Chu; C.T. Yang; N.L. Hsueh, **P.A. Hsiung**, C.S. Koong, “A SysML-based Requirement Supporting Tool for Embedded Software,” *Proceedings of the Fifth International Conference on Secure Software Integration and Reliability Improvement Companion (SSIRI-C, Jeju Island, Korea)*, IEEE CS Press, June 2011.
- [174] Y.-R. Chen, J.-L. Yao, C.-S. Lin, S.-W. Lin, C.-H. Huang, Y.-P. Hu, **P.-A. Hsiung**, S.-J. Chen, and I.-H. Chou, “SAT-based Verification of Data-Independent Access Control Security Systems,” *Proceedings of the International Conference on Security and Management (SAM, Las Vegas, USA)*, pp. 126-131, CSREA Press, July 2011.
- [175] **P.-A. Hsiung** and C.-H. Huang, “SAHA: A Self-Adaptive Hardware-Software System Architecture for Ubiquitous Computing Applications,” *Proceedings of the International Conference on Reconfigurable Systems and Algorithms (ERSA, Las Vegas, USA)*, pp. 263-272, CSREA Press, July 2011.
- [176] C.-S. Lin, W.-L. Liu, W.-T. Yeh, L.-W. Chang, W.-M. Hwu, S.-J. Chen, and **P.-A. Hsiung**, “A Tiling-Scheme Viterbi Decoder in Software-Defined Radio for GPUs,” *Proceedings of the International Conference on Wireless Communications, Networking and Mobile Computing*, (WiCOM), September 2011.
- [177] C.-Y. Shih, M.-C. Li, C.-S. Lin, **P.-A. Hsiung**, C.-H. Chang, W.C. Chu, N.-L. Hsueh, C. Shih, C.-T. Yang, C.-S. Koong, “Adaptive Performance Monitoring for Embedded Multi-core Systems,” *Proceedings of the International Workshop on Embedded Multicore Systems (ICPP-EMS)*, September 2011.

- [178] H.-L. Chao, Y.-R. Chen, **P.-A. Hsiung**, and S.-J. Chen, “Congestion-Aware Scheduling for NoC-based Reconfigurable Systems,” *Proceedings of the the Design, Automation & Test in Europe (DATE)*, Dresden, Germany, March 2012.
- [179] S.-W. Lin, Y. Liu, **P.-A. Hsiung**, J. Sun, and J. S. Dong, “Automatic Generation of Provably Correct Embedded Systems,” *Proceedings of the 14th International Conference on Formal Engineering Methods (ICFEM)*, Kyoto, Japan, November 2012.
- [180] C.-S. Lin, B.-H. Wang, C.-S. Lin, and **P.-A. Hsiung**, “Synchronization-Aware Dynamic Thread Scheduling for Improving Performance and Saving Energy in Multi-Core Embedded Systems,” *Proceedings of the International Symposium on Parallel Architectures, Algorithms and Programming (PAAP)*, Taipei, Taiwan, December 2012.
- [181] C.-T. Ye, T.-D. Wu, Y.-R. Chen, P.-A. He, P.-Q. Xie, Y.-Y. Zhang, S.-M. Teng, Y.-T. Chen, **P.-A. Hsiung**, “Smart Video Camera Design - Real-Time Automatic Person Identification,” *Proceedings of the International Computer Symposium (ICS)*, Hualien Taiwan, December 2012.
- [182] Y.-R. Chen, Z.-R. Wang, **P.-A. Hsiung**, S.-J. Chen, and M.-H. Tsai, “Backward Probing Deadlock Detection for Networks-on-Chip,” *Proceedings of the 7th International Symposium on Networks-on-Chip (NOCS)*, Tempe, Arizona, April, 2013.
- [183] C.-S. Lin, S.-M. Teng, Y.-T. Chen, **P.-A. Hsiung**, “Real-Time Object Detection for Multi-Camera on Heterogeneous Parallel Processing Systems,” *Proceedings of the 7th International Conference on Complex, Intelligent and Software Intensive Systems (CISIS)*, Taichung, Taiwan, July 2013.
- [184] C.-S. Koong, C.-H. Shih, C.-C. Wu, **P.-A. Hsiung**, “The Architecture of Parallelized Cloud-Based Automatic Testing System,” *Proceedings of the 7th International Conference on Complex, Intelligent and Software Intensive Systems (CISIS)*, Taichung, Taiwan, July 2013.
- [185] C.-H. Lu, C.-S. Lin and **P.-A. Hsiung**, “Reconfigurable Multicore Architecture,” *Proceedings of the IEEE 7th International Symposium on Embedded Multicore/Many-core SoCs (MCSoc)*, Tokyo, Japan, September 2013.
- [186] C.-S. Lin, P.-T. Liu, C.-W. Hsieh, H.-Y. Chang, H.-Y. Chang, and **P.-A. Hsiung**, “Efficient Computational Workload Distribution on Heterogeneous GPUs,” *Proceedings of the International Applied Science and Precision Engineering Conference, (APSEC)*, Nantou, Taiwan, October 2013.
- [187] H.-L. Chao, C.-Y. Peng, C.-C. Wu, K.-S. Huang, C.-H. Lu, J.-S. Shen, and **P.-A. Hsiung**, “Spatio-Temporally-Shared Reconfigurable Fast Fourier Transform Architecture Design,” *Proceedings of the International Conference on Field-Programmable Technology (ICFPT)*, Kyoto, Japan, December 2013.
- [188] S.-W. Lin and **P. A. Hsiung**, “Compositional Synthesis of Concurrent Systems through Causal Model Checking and Learning,” *Proceedings of the 19th International Symposium on Formal Methods, (FM)*, Singapore, May 2014.

- [189] Y.-R. Chen, S.-J. Chen, **P.-A. Hsiung**, and I.-H. Chou, “Unified Security and Safety Risk Assessment – A Case Study on Nuclear Power Plant,” *Proceedings of the 1st IEEE International Conference on Trustworthy Systems and Their Applications*, (TSA), Taichung, Taiwan, June 2014.
- [190] J.-S. Shen, P.A. Hsiung, and J.-M. Lu, “Reconfigurable Network-on-Chip Design for Heterogeneous Multi-Core System Architecture,” *Proceedings of the International Workshop on Dynamic Reconfigurable Network-on-Chip (DRNoC)*, Bologna, Italy, July 2014.
- [191] C.-H. Chang, C.-W. Lu, W.-P. Yang, W. C. Chu, and **P.-A. Hsiung**, “A SysML based Requirement Modeling Automatic Transformation Approach,” *Proceedings of the 8th IEEE International Workshop Quality-Oriented Reuse of Software (QUORS)*, Vasteras, Sweden, July 2014.
- [192] P.-C. Hsieh, Y.-R. Chen, W.-H. Wu, and **P.-A. Hsiung**, “Timing Optimization and Control for Smart Traffic,” *Proceedings of the IEEE International Conference on Internet of Things (iThings)*, pp. 9–16, IEEE Computer Society Press, Taipei, Taiwan, September 2014.
- [193] C.-S. Lin, S.-M. Teng, and **P.-A. Hsiung**, “Auto-Tuning for GPGPU Applications using Performance and Energy Model,” *Proceedings of the International Computer Symposium (ICS)*, Taichung, Taiwan, (Intelligent Systems and Applications) pp. 195–204, IOS Press, December 2014.
- [194] H.-L. Chao and **P.-A. Hsiung**, “Micro-Grid Design Modeling and Prototyping,” *Proceedings of the International Computer Symposium (ICS)*, Taichung, Taiwan, (Intelligent Systems and Applications) pp. 225–234, IOS Press, December 2014.
- [195] H.-L. Chao, and **P.-A. Hsiung**, “Model-Predictive Control Optimization for Cyber-Physical Systems,” *Proceedings of the 1st International Workshop on Cyber-Physical Architectures and Design Methodologies*, India, October 2014.
- [196] **P.-A. Hsiung** and R.-H. Hwang, “Refinement Measures for Engineering Education Accreditation - From a Department Perspective,” *Proceedings of the Annual Conference of the European Society for Engineering Education (SEFI)*, France, June 2015.
- [197] C.-H. Huang, K.-W. Tseng, C.-C. Lin, F.-Y. Lin and **P.-A. Hsiung**, “Virtualization Architecture for NoC-based Reconfigurable Systems,” *Proceedings of the 2nd International Workshop on FPGAs for Software Programmers (FSP)*, September 2015.
- [198] C.-H. Lu, H.-L. Chao, Y.-C. Song, and **P.-A. Hsiung**, “Interference-Aware Batch Memory Scheduling in Heterogeneous Multicore Architecture,” *Proceedings of the International Symposium on VLSI Design, Automation and Test (VSLI-DAT)*, IEEE, April 2016.
- [199] **P.-A. Hsiung**, R.-H. Hwang, and Y.-J. Chen, “Introducing Creativity into Engineering Capstone Courses – A Project-Based Learning Approach,” *Proceedings of the Annual Conference of the European Society for Engineering Education (SEFI)*, Finland, September 2016.
- [200] R.-H. Hwang, J.-J. Wu, **P.-A. Hsiung**, and C.-F. Lai, “Design and Implementation of a Learning Platform for a Computer Science Capstone Course based on Project-based Learning and Creative Thinking,” *Proceedings of the Annual Conference of the European Society for Engineering Education (SEFI)*, Finland, September 2016.

- [201] H.-L. Chao, P.-C. Hsieh, T.-C. Yang, and **P.-A. Hsiung**, “Model Predictive Optimization for Distribution Management in Smart Grids,” *Proceedings of the 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, Italy, October 2016.
- [202] Y.-R. Chen, K.-P. Chen, and **P.-A. Hsiung**, “Dynamic Traffic Light Optimization and Control System using Model-Predictive Control Method,” *Proceedings of the IEEE 19th International Conference on Intelligent Transportation Systems (ITSC)*, Brazil, November 2016.
- [203] C.-H. Huang, K.-W. Tseng, and **P.-A. Hsiung**, “Service-oriented Architecture Design for Virtualization in Network-on-Chip,” *Proceedings of the International Computer Symposium (ICS)*, December 2016.
- [204] K.-S. Huang, Y.-L. Chang, and **P.-A. Hsiung**, “An Efficient and Robust Method for Solving Multi-Objective Constraint-Satisfaction Problems in Cognitive Radio Systems,” *Proceedings of the 26th International Telecommunication Networks and Applications Conference (ITNAC)*, pp. 80–82, December 2016.
- [205] F.-S. Lin, P.-T. Liu, M.-H. Li, and **P.-A. Hsiung**, “Feedback Control Optimization for Performance and Energy Efficiency on CPU-GPU Heterogeneous Systems,” *Proceedings of the 16th International Conference on Algorithms and Architectures for Parallel Processing (ICA3PP)*, LNCS Vol. 10048, Springer Verlag, pp. 388–404, December 2016.
- [206] K.-S. Huang, H.-L. Chao, T.-T. Wu, and **P.-A. Hsiung**, “Performance and Security Oriented Software-Defined Network Interface Design,” *Proceedings of the IEEE International Conference on Consumer Electronics (ICCE)*, Las Vegas, USA, January 2017.
- [207] H.-C. Hsu and **P.-A. Hsiung**, “3Rs of Internationalization: Resistance, Requirement, and Realization,” *Asia-Pacific Association for International Education (APAIE)*, Kaohsiung, Taiwan, March 2017.
- [208] Y.-Y. Lin and **P.-A. Hsiung**, “An Early Warning System for Predicting Driver Fatigue,” *Proceedings of the IEEE International Conference on Consumer Electronics - Taiwan (ICCE-Taiwan)*, Taipei, June 2017.
- [209] S.-F. Chen and **P.-A. Hsiung**, “Landslide Prediction with Model Switching,” *Proceedings of the IEEE International Conference on Dependable and Secure Computing (DSC)*, Taipei, Taiwan, August 2017.
- [210] Y.-H. Wang and **P.-A. Hsiung**, “Analysis of the Social Factors of Creativity in Computer Science Engineering Students,” *Proceedings of the 8th International Conference on Language, Education and Innovation (ICLEI)*, Kuala Lumpur, Malaysia, August 2017.
- [211] T.-C. Yang and **P.-A. Hsiung**, “Model Predictive Optimization for Energy Storage based Smart Grids,” *Proceedings of the International Conference on Computing, Analytics and Networks (ICAN)*, Chandigarh, India, October 2017.
- [212] **P.-A. Hsiung** and C.-C. Lin, “Data Reconstruction for Cyber-Physical Landslide Detection System,” *Proceedings of the 7th International Conference on Electronics, Communications and Networks*, Hualien, Taiwan, November 2017.

- [213] **P.-A. Hsiung** and K.-P. Chen, “Vehicle Collision Prediction under Reduced Visibility Conditions,” *Proceedings of the International Conference on Smart Science (ICSS)*, Miyazu, Kyoto, Japan, March 2018.
- [214] **P.-A. Hsiung** and C.-H. Lin, “Cost Optimization of Electrical Usage with Customizable Comfort Considerations,” *Proceedings of the IEEE International Conference on Applied System Innovation (ICASI)*, Chiba, Tokyo, Japan, April 2018.
- [215] H. Tampubolon and **P.-A. Hsiung**, “Supervised Deep Learning Based for Traffic Flow Prediction,” *Proceedings of the International Conference on Smart-Green Technology in Electrical and Information Systems (ICSGTEIS)* Kuta, Badung, Bali, Indonesia, October 2018.

(D) Local Conference Papers

- [216] **P.-A. Hsiung** and S.-J. Chen, “Object-Oriented Synthesis Application Tool,” in *Proceedings of the Fourth Workshop on Object-Oriented Technology*, Taipei, Taiwan, September 1994.
- [217] **P.-A. Hsiung**, T.-Y. Lee, and S.-J. Chen, “A Cosynthesis Methodology for Application-Oriented General-Purpose Parallel Systems,” in *Proceedings of the National Computer Symposium*, Taiwan, Vol. 2, pp. C-76–C-81, December 1997.
- [218] **P.-A. Hsiung**, “Formalizing Hardware-Software Codesign Space Exploration,” in *Proceedings of the 10th VLSI Design/CAD Symposium*, pp. 19-22, Taiwan, August 1999.
- [219] S.-K. Huang, **P.-A. Hsiung**, F. Wang, Y.-S. Kuo, S.-C. Pan, “Verification of Object-Oriented Real-Time Scheduling Systems,” in *Proceedings of the 10th OOTSIG Workshop on Object-Oriented Technology and Applications*, NCTU, Taiwan, pp. 112-117, October 1999.
- [220] **P.-A. Hsiung**, “MRASM: A Multi-Level Rule-Based Architectural Synthesis Methodology for Hierarchically Clustered Parallel Systems,” in *Proceedings of the National Computer Symposium (NCS’99)*, Taiwan, Vol. A, pp. A-487–A-494, December 1999.
- [221] **P.-A. Hsiung**, “Object-Oriented Technology Transfer to Hardware-Software Codesign of Embedded Real-Time Systems,” in *Proceedings of the 11th OOTSIG Workshop on Object-Oriented Technology and Applications (THU, Taiwan)*, pp. C-14 – C-21, September 2000.
- [222] W.-B. See, S.-J. Chen, **P.-A. Hsiung**, and T.-Y. Lee, “Tunable Embedded Software Development Platform,” in *Proceedings of the National Computer Symposium (NCS’01, Taiwan)*, pp. G110–G116, December 2001.
- [223] W.-B. See, **P.-A. Hsiung**, and S.-J. Chen, “Tunable Embedded System Development Platform,” in *Proceedings of the 2002 VLSI Design / CAD Symposium (VLSI’02, Taitung, Taiwan)*, pp. 532-535, August 2002.
- [224] W.-B. See, **P.-A. Hsiung**, T.-Y. Lee, and S.-J. Chen, “Modular Mobile Dispatching System (MMDS) and Logistics,” in *Proceedings of the 2002 Annual Conference on National Defense Integrated Logistics Support (ILS, Taipei, Taiwan)*, pp. 365-371, August 2002.
- [225] **P.-A. Hsiung**, S.-Y. Cheng, and T.-Y. Lee, “Compositional Verification of Synchronous Real-Time Embedded Systems,” in *Proceedings of the 2002 VLSI Design / CAD Symposium (VLSI’02, Taitung, Taiwan)*, pp. 187-190, August 2002.

- [226] **P.-A. Hsiung**, W.-B. See, and T.-Y. Lee, “An Object-Oriented Application Framework for Verifiable Embedded Real-Time Software,” in *Proceedings of the 13th Workshop on Object-Oriented Technology and Applications (OOTSIG’2002, Taichung, Taiwan)*, pp. 273–280, September 2002.
- [227] W.-B. See, **P.-A. Hsiung**, T.-Y. Lee, and S.-J. Chen, “Verification of Embedded Object-Oriented Software,” in *Proceedings of the 13th Workshop on Object-Oriented Technology and Applications (OOTSIG’2002, Taichung, Taiwan)*, pp. 281–284, September 2002.
- [228] W.-S. Liao and **P.-A. Hsiung**, “Modeling Hardware Systems with Complex Clock Synchronizations in the SGM Formal Verifier,” in *Proceedings of the VLSI Design / CAD Symposium, Hwalien, Taiwan, August 2003*.
- [229] H.-C. Kao, **P.-A. Hsiung**, T.-Y. Lee, J.-M. Fu, and W.-B. See, “A UML-Based Synthesis and Verification Framework for Real-Time Embedded Software,” in *Proceedings of the 14th Workshop on Object-Oriented Technology and Applications*, pp. 25–32, September 2003.
- [230] T.-Y. Lee, I.-M. Wu, **P.-A. Hsiung**, C.-P. Chang, C.-C. Tsai, and W.-T. Lee, “Design of a Software Synthesis Tool for Real-Time Embedded Systems,” in *Proceedings of the 14th Workshop on Object-Oriented Technology and Applications*, pp. 609–616, September 2003.
- [231] W.-B. See, J.-W. Yang, **P.-A. Hsiung**, and S.-J. Chen, “Multiple-Protocol Mobile Data Terminal for Logistic Dispatching Applications,” in *Proceedings of the 2003 Annual Conference on National Defense Integrated Logistics Support*, pp. 348–353, October 2003.
- [232] W.-S. Liao, M.-H. Sun, W.-C. Chao, C.-C. Wu, T.-C. Li, W.-Y. Tsai, and **P.-A. Hsiung**, “A Formal Verification Platform for AMBA-based SoCs,” in *Proceedings of the VLSI Design / CAD Symposium, Taiwan, August 2004*.
- [233] **P.-A. Hsiung**, C.-F. Liao, C.-H. Tseng, S.-W. Lin, Y.-H. Chen, and K.-L. Chiu, “Hardware-Software Codesign and Coverification Methodology for Dynamically Reconfigurable System-on-Chips,” in *Proceedings of the 15th Workshop on Object-Oriented Technology and Applications (OOTSA’2004)*, September 2004.
- [234] **P.-A. Hsiung**, “Real-Time Embedded Software Engineering,” in *Proceedings of the 1st Taiwan Software Engineering Conference (TSEC’2005)*, pp. 347–352, June 2005.
- [235] C.-H. Tseng and **P.-A. Hsiung**, “UML-based Rapid Prototyping Design Flow for Dynamically Reconfigurable Computing Systems,” in *Proceedings of the VLSI Design / CAD Symposium, August 2005*.
- [236] C.-F. Liao and **P.-A. Hsiung**, “A SystemC-based Performance Evaluation Framework for Dynamically Reconfigurable SoC,” in *Proceedings of the VLSI Design / CAD Symposium, August 2005*.
- [237] C.-H. Huang, S.-S. Chang, and **P.-A. Hsiung**, “Generic Wrapper Design for Dynamic Swappable Hardware IP in Partially Reconfigurable Systems,” in *Proceedings of the VLSI Design / CAD Symposium, August 2006*. (Invited for Journal Publication in the International Journal of Electrical Engineering)

- [238] C.-C. Hung and **P.-A. Hsiung**, “Reconfigurable Hardware Module Sequencer for Dynamically Partially Reconfigurable Systems,” in *Proceedings of the VLSI Design / CAD Symposium*, August 2007.
- [239] **P.-A. Hsiung** and S.-W. Lin, “Verifiable Embedded Real-Time Application Framework,” in *Proceedings of the Workshop on Open-Source Technology and Applications* (Taipei, Taiwan), November 2007 (invited for presentation).
- [240] C. Yu, M.-H. Yen, **P.-A. Hsiung**, and S.-J. Chen, “A Unified Block Interleaving/Deinterleaving Architecture for Wireless Communication Applications,” in *Proceedings of the VLSI Design / CAD Symposium*, August 2008.
- [241] P.-H. Lu and **P.-A. Hsiung**, “Dynamically Switching Between Hardware Abstraction Models for Rapid Embedded Software Development,” in *Proceedings of the VLSI Design / CAD Symposium*, August 2008.
- [242] C.-H. Lu, H.-W. Liao, and **P.-A. Hsiung**, “Multi-Objective Placement of Reconfigurable Hardware Tasks in Real-Time Systems,” in *Proceedings of the VLSI Design / CAD Symposium*, August 2008.
- [243] J.-S. Shen, W.-W. Lin, and **P.-A. Hsiung**, “Efficiently Reconfigurable NoC with Operating System Support,” in *Proceedings of the Conference on Innovative Applications of System Prototyping and Circuit Design*, October 2008. Best Paper Award (3 best paper awards out of 77 submissions)
- [244] C.-H. Huang, J.-S. Shen, and **P.-A. Hsiung**, “Model-Based Verification and Estimation Framework for Dynamically Partially Reconfigurable System,” in *Proceedings of the National Computer Symposium* (NCS, Taiwan), December 2009. (*Best Paper Award in the Workshop on Computer Architecture, Embedded Systems, and VLSI/EDA*)
- [245] Y.H. Lin, S.W. Lin, C.S. Lin, C.H. Lu, S.Y. Tong, B.H. Wang, C.C. Ho, Y.L. Chang, and **P.-A. Hsiung**, “Synthesis and Code Generation of Multi-Core Embedded Software,” in *Proceedings of the Joint Conference on Object-Oriented Technology and Applications* (OOTA) and *Software Engineering* (TCSE), July 2010.
- [246] C.-H. Huang, J.-S. Shen, and **P.-A. Hsiung**, “Self-Adaptive Hardware-Software Architecture for Embedded and Ubiquitous Systems,” in *Proceedings of the VLSI Design / CAD Symposium*, August 2010.
- [247] S.-S. Lu, C.-H. Lu, and **P.-A. Hsiung**, “Congestion- and Energy-Aware Run-Time Mapping for Tile-Based Network-on-Chip Architecture,” in *Proceedings of the VLSI Design / CAD Symposium*, August 2010.
- [248] B.-H. Wang and **P.-A. Hsiung**, “Dynamic Thread Scheduling on MP-SoC using Game Theory,” in *Proceedings of the VLSI Design / CAD Symposium*, August 2010.
- [249] H.-L. Chao, S.-Y. Tung, **P.-A. Hsiung**, “Congestion-Aware Scheduling for NoC-based Reconfigurable Systems,” in *Proceedings of the VLSI Design / CAD Symposium*, August 2011.

- [250] P.-Y. Tsai, H.-Y. Yeh, T.-S. Hsu, S.-Y. Pan, L.-W. Sung, B. Kumar, and **P.-A. Hsiung**, "A Multicore System Design for Basketball Detection and Tracking in Sports Competition Video Streaming," in *Proceedings of the Workshop on Consumer Electronics*, Taiwan, November 2011.
- [251] C.-H. Huang and **P.-A. Hsiung**, "Virtualizable Hardware/Software Design Infrastructure for Dynamically Partially Reconfigurable Systems," in *Proceedings of the VLSI Design / CAD Symposium*, August 2012.
- [252] H.-L. Chao, C.-C. Tsai, W.-H. Wu, P.-C. Hsieh, Y.-R. Chen, **P.-A. Hsiung**, and I.-H. Chou, "Design Optimization for Demand-Response in Renewable Energy Source Micro-Grids," in *Proceedings of the 9th Intelligent Living Technology Conference (ILT)*, June 2014. (in Chinese)
- [253] W.-H. Wu, P.-C. Hsieh, Y.-R. Chen, and **P.-A. Hsiung**, "The Dynamic Setting of Traffic Lights and Optimization in Smart City," in *Proceedings of the International Conference on Information Management (ICIM)*, May 2014. (in Chinese)
- [254] C.-H. Lu, C.-S. Lin, and **P.-A. Hsiung**, "A Software Defined Radio Case Study for Reconfigurable Multicore Architecture," in *Proceedings of the VLSI Design/CAD Symposium*, August 2014.
- [255] C.-Y. Wang, C.-H. Huang, and **P.-A. Hsiung**, "Elastic Superposition Mapping for Heterogeneous Tasks in Reconfigurable Multicore Architecture," in *Proceedings of the VLSI Design/CAD Symposium*, August 2014.
- [256] K.-P. Chen and **P.-A. Hsiung**, "Dynamic Vehicle Rear-End Collision Prediction System," in *Proceedings of the VLSI Design/CAD Symposium*, August 2017.
- [257] S.-F. Chen and **P.-A. Hsiung**, "Landslide Prediction with Model Switching," in *Proceedings of the VLSI Design/CAD Symposium*, August 2017.

(E) Technical Reports and Others

- [258] F. Wang and **P.-A. Hsiung**, "Parametric Analysis of Computer Systems," *Technical Report TR-IIS-97-010*, Institute of Information Science, Academia Sinica, Taiwan, 1997.
- [259] **P.-A. Hsiung**, Farn Wang, and Yue-Sun Kuo, "Scheduling System Verification," *Technical Report TR-IIS-98-014*, Institute of Information Science, Academia Sinica, Taiwan, 1998.
- [260] F. Wang and **P.-A. Hsiung**, "Iterative Refinement and Condensation for State-Graph Construction," *Technical Report TR-IIS-98-009*, Institute of Information Science, Academia Sinica, Taiwan, 1998.
- [261] **P.-A. Hsiung**, J.-M. Fu, T.-Y. Shen, C.-Y. Lin, L.-M. Chen, and H.-C. Gao, "A Verifiable Embedded Real-Time Application Framework," In *Proc. of the Annual Workshop on Intelligent Wireless Mobile Applications*, Chinese Military Academy, Taiwan, May 2003.
- [262] **P.-A. Hsiung**, J.-M. Fu, T.-Y. Shen, C.-Y. Lin, L.-M. Chen, and H.-C. Gao, "VERTAF: Verifiable Embedded Real-Time Application Framework," *Electron Technology Information Magazine*, Volume 33, Gal-Lant Co. Ltd., Taiwan, September 2003.

- [263] C.-H. Tseng and **P.-A. Hsiung**, “Hardware-Software Codesign of Reconfigurable Computing Systems using Java and UML,” *Electron Technology Information Magazine*, Volume 53, pp. 21–26, Gal-Lant Co. Ltd., Taiwan, May 2005. (in Chinese)
- [264] C.-H. Huang, S.-H. Chang, and **P.-A. Hsiung**, “Reconfigurable Digital Camera Design,” *Electron Technology Information Magazine*, Volume 56, pp. 19–23, Gal-Lant Co. Ltd., Taiwan, August 2005. (in Chinese)
- [265] S.-W. Lin, C.-H. Hwang, C.-H. Tseng, C.-F. Liao, and **P.-A. Hsiung**, “Hardware-Software Codesign of Reconfigurable Systems-on-Chip,” *Electron Technology Information Magazine*, Volume 57, pp. 38–43, Gal-Lant Co. Ltd., Taiwan, September 2005. (in Chinese)
- [266] C.-W. Liu, C.-H. Hwang, H.-C. Kao, and **P.-A. Hsiung**, “Low-Power Scheduling for Real-Time Embedded Systems,” *Electron Technology Information Magazine*, Volume 60, pp. 16–20, Gal-Lant Co. Ltd., Taiwan, December 2005. (in Chinese)
- [267] C.-H. Hwang, and **P.-A. Hsiung**, “Hardware-Software Codesign of SoC,” *Electron Technology Information Magazine*, Volume 60, pp. 37–41, Gal-Lant Co. Ltd., Taiwan, December 2005. (in Chinese)
- [268] S.-H. Chang and **P.-A. Hsiung**, “Operating System Design for Reconfigurable Systems,” *Electron Technology Information Magazine*, Volume 64, pp. 20–26, Gal-Lant Co. Ltd., Taiwan, April 2006. (in Chinese)
- [269] C.-W. Liu, C.-F. Liao, and **P.-A. Hsiung**, “SystemC-based Performance Evaluation Framework for Dynamically Reconfigurable System-on-Chip,” *Electron Technology Information Magazine*, Volume 64, pp. 40–44, Gal-Lant Co. Ltd., Taiwan, April 2006. (in Chinese)
- [270] H.-W. Liao and **P.-A. Hsiung**, “Configurable Real-Time Embedded Operating System,” *Electron Technology Information Magazine*, Volume 65, pp. 40–44, Gal-Lant Co. Ltd., Taiwan, May 2006. (in Chinese)
- [271] Y.-R. Chen, Y.-H. Lin, and **P.-A. Hsiung**, “Model Checking Safety-Critical Systems using Safecharts,” *Electron Technology Information Magazine*, Volume 66, pp. 41–45, Gal-Lant Co. Ltd., Taiwan, June 2006. (in Chinese)
- [272] **P.-A. Hsiung**, J.-Y. Chien, C.-Y. Wu, and G.-H. Lin, “RFID-based Automation of Airport Baggage Handling,” *Electron Technology Information Magazine*, Volume 68, pp. 36–40, Gal-Lant Co. Ltd., Taiwan, August 2006. (in Chinese)
- [273] **P.-A. Hsiung**, “Real-Time Embedded Software Tool Design,” *Engineering Science and Technology Bulletin*, Vol. 87, pp. 38–41, National Science Council, Taiwan, August 2006. (in Chinese)
- [274] S.-J. Chen, **P.-A. Hsiung**, T.-Y. Lee, J.-S. Cherng, and M.-H. Yen, “Tunable SoC Hardware-Software Development Platform,” *Engineering Science and Technology Bulletin*, Vol. 87, pp. 107–117, National Science Council, Taiwan, August 2006. (in Chinese)
- [275] **P.-A. Hsiung**, “Design and Implementation of a Real-Time Operating System for Scalable Low-Power Customized Embedded Systems,” *Engineering Science and Technology Bulletin*, Vol. 94, pp. 89–93, National Science Council, Taiwan, October 2007. (in Chinese)

- [276] C.-Y. Hsu, M.-C. Chiu, S.-C. Lee, K.-C. Chiang, C.-C. Tsao, **P.-A. Hsiung**, “Postal R Generation – RFID-based Postal Revolution,” RFID Workshop, Taipei, Taiwan, January 2008. (in Chinese)
- [277] C.-T. Ho, N.-F. H, C.-J. Lin, M.-M. Chao, K.-C. Chiang, C.-C. Tsao, and **P.-A. Hsiung**, “RFID-based Traffic Control System,” RFID Workshop, Taipei, Taiwan, January 2008. (in Chinese)

11 Tool and Software Developments

Dr. Hsiung has designed and implemented various system design and verification tools, including SGM, VERTAF, PLX OS, and FVP. SGM is a compositional model checker for real-time systems, including both hardware and software. VERTAF is an application framework for the design and verification of real-time embedded software. PLX OS is a simple operating system for the PLX processor. FVP is a formal verification platform for Systems-on-Chip (SoC) based on the SGM model checker.

1. **SGM**: (State-Graph Manipulators) The development of SGM, a compositional model checker for concurrent real-time systems, started from July 1997. It was a three year project in collaboration with Dr. Farn Wang, who was with Academia Sinica, Taipei at that time and is currently with the National Taiwan University. SGM has undergone various development phases, including its adaptation for assume-guarantee reasoning, for SoC verification, for multi-clock synchronization semantics, for mutation coverage, and for priority systems. The tool now consists of more than 45,000 lines of C code, with a user-friendly graphical interface. It is currently licensed for use by more than 350 parties from more than 30 countries around the world. Both industry and academia people are using the tool for technology experiments and verification research. It has also been included in various popular known tool lists such as the *Formal Methods Virtual Library*. Current version SGM v2.0 can be downloaded at ["http://www.cs.ccu.edu.tw/~pahsiung/sgm/"](http://www.cs.ccu.edu.tw/~pahsiung/sgm/).
2. **VERTAF**: (Verifiable Embedded Real-Time Application Framework) VERTAF is a component-based application framework for the modeling, design, and verification of real-time embedded software. Three technologies are integrated in VERTAF, namely software component reuse, formal synthesis, and formal verification. This is a 3-year long-term project spanning years 2002 to 2005, funded by the National Science Council, Taiwan. The results of this project has been published in the *IEEE Transactions on Software Engineering*, Vol. 30, No. 10, October 2004, and other well-known journals. The tool is currently available as open source at the Open Foundry website ["http://of.openfoundry.org/projects/610/download"](http://of.openfoundry.org/projects/610/download). The tool is now being extended to support multicore processor programming.
3. **PLX OS**: This is a simple operating system for the PLX processor. It consists a priority scheduler with round-robin scheduling for equal priority tasks. It has a memory manager, a locator, and a loader. It is available in open source from ["http://www.cs.ccu.edu.tw/~pahsiung/plxos/"](http://www.cs.ccu.edu.tw/~pahsiung/plxos/).

4. **FVP:** (Formal Verification Platform) A model-checking platform for Systems-on-Chip (SoCs). Currently, FVP supports ARM's AMBA and IBM's Coreconnect bus-based SoC architectures. Implemented technologies include extended timed automata models for each bus component (master, slave, arbiter, bridge), compositional model checking, functional abstraction, transaction-level verification, semi- or dynamic formal verification, and coverage estimations for a set of TCTL properties in model checking. This platform is based on SGM and has been successfully applied to SoCs.

12 Invited Tutorials and Short Courses

1. "Application of RFID Technology to Special Education," National Chiayi School of Special Education, Chiayi, Taiwan, November 5 and 7, 2008 (Invited 5 hours Short Course).
2. "Formal Verification," National Taichung University, Department of Computer and Information Science, Taichung, Taiwan, August 28 and September 4, 2008 (Invited 10 hours Short Course).
3. "Embedded Operating System Design for SIMD Processors," IEEE SoC Conference (SOCC), Invited Tutorial, Hsinchu, Taiwan, September 28, 2007.
4. "Embedded Software Design," Tze-Chiang Foundation of Science and Technology, Hsin-Chu, Taiwan, March 4, 5, 18, 19, 2006 (Invited 24-hours Tutorial Course).
5. "Embedded Software Design," Tze-Chiang Foundation of Science and Technology, Hsin-Chu, Taiwan, January 7, 8, 21, 22, 2006 (Invited 24-hours Tutorial Course).
6. "Embedded Software Design," Tze-Chiang Foundation of Science and Technology, Hsin-Chu, Taiwan, June 18, 19, July 2, 3, 2005 (Invited 30-hours Tutorial Course).
7. "Digital Camera Chipset Design and Verification," Tze-Chiang Foundation of Science and Technology, Hsin-Chu, Taiwan, January 7, 2005 (Invited Full-Day Tutorial).
8. "Design and Verification of Digital Camera SoC," Tze-Chiang Foundation of Science and Technology, Hsin-Chu, Taiwan, June 29, 2004 (Invited Full-Day Tutorial).
9. "Introduction to Hardware-Software Codesign," Tze-Chiang Foundation of Science and Technology, Hsin-Chu, Taiwan, February 29, 2004 (Invited Full-Day Tutorial).
10. "Design Verification for System-on-Chip," Tze-Chiang Foundation of Science and Technology, Hsin-Chu, Taiwan, January 31, February 10, and February 28 2004 (Invited 3-Day Tutorials).
11. "System-on-Chip Design," Tze-Chiang Foundation of Science and Technology, Hsin-Chu, Taiwan, January 10, 2004 (Invited Full-Day Tutorial).

12. "Verification and Validation of Mobile Applications," Summer Course on Wireless Mobile Applications, Department of Electrical Engineering, National Chung Cheng University, Chiayi, Taiwan, July 28, 29, 2003.
13. "Embedded Software Design," Tecom Company Ltd., Hsin-Chu, Taiwan, March 28, 2003 (Invited Half-Day Tutorial).
14. "Embedded Software Design," Tze-Chiang Foundation of Science and Technology, Hsin-Chu, Taiwan, February 21, 2003 (Invited Full-Day Tutorial).
15. "Hardware-Software Co-design," Tze-Chiang Foundation of Science and Technology, Educational Training Center, Taipei, Taiwan, October 4, 2002 (Invited Full-Day Tutorial).
16. "Embedded System Design," Tze-Chiang Foundation of Science and Technology, Educational Training Center, Taipei, Taiwan, September 27, 2002 (Invited Full-Day Tutorial).

13 Invited Talks

1. "Model Predictive Optimization for Smart Grid Design," Department of Software Engineering and Management, National Kaohsiung Normal University, June 2017.
2. "The 3Rs of Internationalization," English Language Teaching and Learning Conference, May 20, 2017.
3. "The Rise of Artificial Intelligence," National Chung Cheng University, May 2017.
4. "Reconfigurable Network-on-Chip Design," Department of Computer Science, National University of Singapore, August 2013.
5. "SAT-based Formal Verification of Security Systems," Temasek Laboratories, National University of Singapore, August 2013.
6. "Reconfigurable Network-on-Chip Design," Temasek Laboratories, National University of Singapore, August 2013.
7. "Reconfigurable Network-on-Chip Design," Electronic Design Automation Workshop, Taoyuan, Taiwan, December 2012.
8. "SAHA: A Self-Adaptive Hardware-Software System Architecture for Ubiquitous Computing Applications," International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA), Las Vegas, Nevada, USA, July 2011.
9. "Model-driven Development of Multi-core Embedded Software," Department of Computer Science and Information Engineering, National Central University, Taiwan, April 2011.
10. "Model-driven Development of Multi-core Embedded Software," Department of Computer Science, National Cheng-Chi University, Taipei, Taiwan, March 2011.
11. "Learning-based Assume Guarantee Synthesis," 1st Workshop on Automated Verification, Analysis and Synthesis (WAVAS), Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, February 2011.

12. "Reconfigurable System Design," National Taipei University of Technology, Department of Electronic Engineering, Taipei, Taiwan, October 2010.
13. "Reconfigurable Network-on-Chip Design," National Tai-Tung University, Department of Computer Science and Information Engineering, Taitung, Taiwan, May 2010.
14. "Reconfigurable Network-on-Chip," National Chiao Tung University, Department of Computer Science and Information Engineering, Hsinchu, Taiwan, May 2010.
15. "Model-Driven Multi-Core Embedded Software Design," Feng Chia University, Department of Computer Science and Information Engineering, Taichung, Taiwan, April 2010.
16. "Reconfigurable Computing," National Taipei University of Technology, Department of Electronic Engineering, Taipei, Taiwan, November 5, 2009.
17. "Low Power Scheduling for Embedded Systems using Real-Time Petri Nets," Artificial Intelligence Forum, Taipei, Taiwan, May 16, 2009.
18. "Model Checking Safety-Critical Systems using Safecharts," National Taiwan Normal University, Department of Computer Science and Information Engineering, Taipei, Taiwan, December 17, 2008.
19. "Reconfigurable System Design using FPGA," Kun Shan University, Department of Electronic Engineering, Tainan, Taiwan, November 25, 2008.
20. "Reconfigurable System Design using FPGA," National Taiwan University of Science and Technology, Department of Electronics Engineering, Taipei, Taiwan, November 24, 2008.
21. "Synchronous Distance Learning Techniques," Workshop on Distance Learning Course Design and Certification, E-Learning Center, National Chung Cheng University, July 16, 2008.
22. "Information Engineering and Me!" CCU-CSIE Camp, National Chung Cheng University, July 7, 2008.
23. "Modeling and Formal Analysis of Safety-Critical Systems using Extended Safecharts," The 4th Taiwanese-French Conference on Information Technology (TFIT), Taipei, Taiwan, March 3, 2008.
24. "VERTAF: Verifiable Embedded Real-Time Application Framework," Tung-Hai University, Department of Computer Science and Information Engineering, Taichung, Taiwan, January 18, 2008.
25. "Reconfigurable System Design," National Pingtung Institute of Commerce (NPIC), Department of Information Technology, Pingtung, Taiwan, November 30, 2007.
26. "Reconfigurable System Design and Verification," National Taiwan University of Science and Technology, Taipei, Taiwan, October 22, 2007.
27. "Reconfigurable Hardware Design," National Changhua University of Education, Department of Electronics Engineering, Changhua, Taiwan, June 22, 2007.
28. "System-Level Design using SystemC," Graduate Institute of Electronic Engineering, National Taiwan University, Taipei, Taiwan, April 3, 2007.

29. "Dynamically Reconfigurable Hardware-Software Systems," Department of Computer Science and Information Engineering, National Changhua University of Education, Changhua, Taiwan, April 18, 2006.
30. "Dynamically Reconfigurable Hardware-Software Systems," Department of Computer Science and Information Engineering, Chao-Yang Technical University, Taichung, Taiwan, March 28, 2006.
31. "Hardware-Software Codesign Techniques for Reconfigurable Systems," Department of Computer Science and Engineering, National Sun Yat Sen University, Kaohsiung, Taiwan, March 10, 2006.
32. "Case Studies on Software Failures," Software Engineering and Quality Workshop, Southern Taiwan University of Technology, Department of Computer Science and Information Engineering, Tainan, Taiwan, December 2, 2005.
33. "Hardware-Software Codesign of Dynamically Reconfigurable Systems," National Taipei University of Technology, Department of Electronic Engineering, Taipei, Taiwan, November 16, 2005.
34. "Dynamically Reconfigurable System-on-Chip Hardware-Software Codesign," National Taiwan University, Department of Computer Science and Information Engineering, Taipei, Taiwan, November 4, 2005.
35. "Hardware-Software Codesign of Dynamically Reconfigurable System-on-Chip," Fu-Jen University, Department of Electronic Engineering, Taipei, Taiwan, September 28, 2005.
36. "Reconfigurable System-on-Chip Design," SoC Design Workshop, Institute of Applied Electronic Technology, National Taiwan Normal University (NTNU), Taiwan, December 31, 2004.
37. "Automatic Synthesis and Verification of Real-Time Embedded Software," National Huwei University of Science and Technology, Department of Computer Science and Information Engineering, Hu-Wei, Taiwan, September 30, 2004.
38. "A Formal Verification Platform for SoC," National Chiao Tung University, Department of Computer and Information Science, Hsinchu, Taiwan, May 25, 2004.
39. "Framework-based Formal Design and Verification of Real-Time Embedded Software," Taiwan-France Research and Technology Collaboration Workshop, Paris, France, April 14–16, 2004.
40. "A Formal Verification Platform for SoC," 3rd Annual Emerging Information Technology Conference (EITC), Princeton University, USA, October 31, 2003.
41. "Co-design Models, Architectures, and Specification Languages," Department of Electrical Engineering, National Taiwan University, Taipei, February 25, 2003.
42. "Formal Methods for Real-Time Embedded Software Engineering," Department of Computer Science, National Tsing-Hua University, Hsinchu, May 22, 2002.
43. "Automatic Synthesis and Code Generation of Real-Time Embedded Software," Department of Electrical Engineering, National Cheng-Kung University, Tainan, April 26, 2002.
44. "Formal Verification of SoC," Department of Electrical Engineering, National Taiwan University, Taipei, March 25, 2002.

45. “Real-Time Embedded Software Synthesis,” Department of Electrical Engineering, Da-Yeh University, Chang-Hua, March 18, 2002.
46. “Current Research Work,” IICM Annual Meeting, K.T. Li Research Awarding Ceremony, National Taiwan University, Taipei, January 26, 2002.
47. “Real-Time Embedded Software Synthesis,” Department of Electrical Engineering, Chung Cheng Institute of Technology, National Defense University, Taoyuan, November 29, 2001.
48. “Compositional Verification of Concurrent Real-Time Systems,” Department of Computer Science and Information Engineering, Fu-Jen Catholic University, Hsin-chuang, Taiwan, May 17, 2000.
49. “Compositional Verification of Concurrent Real-Time Systems,” Department of Computer Science and Information Engineering, National Chung-Cheng University, Chiayi, Taiwan, May 3, 2000.
50. “Compositional Verification of Concurrent Real-Time Systems,” Department of Computer Science and Information Engineering, Tatung University, Taipei, Taiwan, April 17, 2000.
51. “Compositional Verification of Concurrent Real-Time Systems,” Department of Computer Science and Information Engineering, National Chi-Nan University, Nantou, March 16, 2000.
52. “Compositional Verification of Concurrent Real-Time Systems,” *Graduate Seminar Talk*, Graduate Institute of Computer Science and Information Engineering, National Taiwan University, Taipei, March 10, 2000.
53. “A Case Study in Hardware-Software Codesign – Vehicle Parking Management System,” *Graduate Seminar Talk*, Graduate Institute of Electrical Engineering, Tamkang University, Taipei, December 6, 1999.
54. “User Friendly Verification,” *Graduate Seminar Talk*, Graduate Institute of Electrical Engineering, Tamkang University, Taipei, December 6, 1999.
55. “Hardware-Software Codesign and Coverification,” *Graduate Seminar Talk*, Graduate Institute of Electrical Engineering, Chang-Keng University, Kwei-Shan, Taiwan, March 15, 1999.
56. “User-Friendly Verification,” *Graduate Seminar Talk*, Graduate Institute of Computer Science and Information Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan, March 9, 1999.
57. “SGM: A User-Friendly Verification Environment,” *3rd Joint Seminar on Programming Languages and Systems*, National Taiwan University and Institute of Information Science, Academia Sinica, March 5, 1999.

14 Journal Editorships

14.1 Editorial Board Member of several journals

1. Editorial Board Member, Advance in Environmental Waste Management and Recycling (AEWMR), OPAST Group LLC, since 2018.

2. Associate Editor for Far East, International Journal of Computational Complexity and Intelligent Algorithms (IJCCIA), since 2017.
3. Editor-in-Chief, Software Engineering Topic, *International Journal of Advances in Computing Technology* (IJACT), Advanced Institute of Convergence IT, since 2011.
4. Editor-in-Chief, Automated Control Systems Topic, *International Journal of Intelligent Information Processing* (IJIIP), Human and Sciences Publication, since 2011.
5. Editorial Board Member, *Open Conference Proceedings Journal*, Bentham Open, USA, since 2014.
6. Editorial Board Member, *Current Advances in Artificial Intelligence* (CAAI), American V-King Scientific Publishing, LTD, USA, since 2013.
7. Associate Editor, *Aloy Journal of Soft Computing and Applications* (AJSCA), Aloy Publishers, USA, since 2013.
8. Editorial Board Member, *International Journal of Circuits and Architecture Design* (IJCAD), Inderscience Publishers, USA, since 2013.
9. Editor, *Universal Journal of Software Engineering*, Prakriti Publications, India, 2013 ~ 2016.
10. Editor, *Journal of Circuit, Architecture and Design*, IDOSI, India, since 2012.
11. Editor, *Conference Papers in Computer Science*, Hindawi Publishing Corporation, USA, (<http://www.cpis.com/journals/cs/>), since 2012.
12. Editor, *International Journal of Next Generation Information Technology* (JNIT), Human and Sciences Publication, since 2011.
13. Editor, *International Journal of Advances in Information Sciences and Service Sciences* (AISS), Advanced Institute of Convergence IT, since 2011.
14. Editor, *International Journal of Embedded Systems* (IJES), Inderscience Publishers, USA, (<http://www.inderscience.com>), since 2003.
15. Associate Editor, *Journal of Software Engineering* (JSE), Academic Journals, Inc., USA, (<http://www.academicjournals.net>), since 2006.
16. Editorial Board Member, *Open Computer Science Journal*, Bentham Science Publishers, Ltd., USA, (<http://www.bentham.org/>) since 2014.
17. International Editorial Board Member, *International Journal of Patterns* (IJOP), USA, (<http://www.ijop.org/>), June 2007 ~ now.
18. Editorial Board Member, *International Journal of Multimedia and Ubiquitous Engineering* (IJMUE), Science and Engineering Research Center (SERSC), USA, (<http://www.sersc.org/>) since 2007.

14.2 Guest Editing Journal Special Issues

1. Editorial Member, Special Issue on “Hardware/Software Support for High Performance Scientific and Engineering Computing,” *IEICE Transactions on Information and Systems*, 2004.

2. Guest Editor, Special Issue on “Hardware-Software Codesign of System-on-Chips,” *International Journal of Embedded Systems (IJES)*, Vol. 1, No. 1/2, Inderscience Publishers, USA, 2005.
3. Guest Editor, Special Issue on “Real-Time Embedded Software,” *International Journal of Embedded Systems (IJES)*, Vol. 2, No. 3/4, Inderscience Publishers, USA, 2006.
4. Guest Editor, Special Issue on “Reconfigurable and Multi-Core Embedded Systems,” *International Journal of Embedded Systems (IJES)*, Vol. 4, No. 3/4, Inderscience Publishers, USA, 2010.
5. Guest Editor, Special Issue on “Embedded Multicore Systems: Architecture, Performance and Application,” *Microprocessors and Microsystems*, Elsevier, 2012.
6. Guest Editor, Special Issues for The International Workshop on Bioinformatics and Ubiquitous Computing, *Computers and Electrical Engineering*, Computing and Informatics (SCI journals) to be published in 2013.
7. Guest Co-Editor, Special Issue on Programming and Architecture Support for Embedded Multicore SoC Systems, *International Journal of Adaptive and Innovative Systems (IJASIS)* InderScience publishers, to be published in 2014.
8. Guest Co-Editor, Special issue on Embedded Multicore and Many-core Architectures, *International Journal of Embedded Systems (IJES)*, Inderscience publishers, to be published in 2014.

15 Conference Program Committee Member

Dr. Hsiung has served in several program committees of international conferences and workshops.

1. PDPTA'99 (*International Conference on Parallel and Distributed Processing Techniques and Applications*), Las Vegas, Nevada, USA, June-July 1999.
2. RTC'99 (International Workshop on Real-Time Constraints), Alexandria, Virginia, USA, October 1999.
3. DSVV'2000 (International Workshop on Distributed System Validation and Verification), Taipei, Taiwan, April 2000.
4. PDPTA'2000 (*International Conference on Parallel and Distributed Processing Techniques and Applications*), Las Vegas, Nevada, USA, June 2000.
5. SPDSEC'2002 (*The 1st Workshop on Hardware/Software Support for Parallel and Distributed Scientific and Engineering Applications*), PACT Workshop, USA, September 2002.
6. ICS'2002 (*International Computer Symposium*), International Workshop on Computer Systems, Taipei, December 2002.
7. RTCSA'2003 (*The 9th International Conference on Real-Time and Embedded Computing Systems and Applications*), Tainan, Taiwan, February 2003.
8. SHPSEC'2003, (*The 2nd Workshop on Hardware/Software Support for High Performance Scientific and Engineering Computing*), in conjunction with *The 12th International Conference on Parallel Architectures and Compilation Techniques* (PACT-03), USA, September 2003.

9. AANET'2003 (*International Workshop on Applications of Ad Hoc Networks*), Kaohsiung, Taiwan, October 2003.
10. ATVA'2003 (*The 1st Workshop on Automated Technology for Verification and Analysis*), National Taiwan University, Taipei, Taiwan, December 2003.
11. EC'2004 (*The 1st International Workshop on Embedded Computing*), In conjunction with ICDCS'2004, Tokyo, Japan, March 2004.
12. EUC'2004 (*International Conference on Embedded and Ubiquitous Computing*), Aizu, Japan, August 26-28, 2004.
13. ATVA'2004 (*The 2nd International Symposium on Automated Technology for Verification and Analysis*), National Taiwan University, Taipei, Taiwan, October 2004.
14. IEHSC'2005 (*International Embedded and Hybrid Systems Conference*), Singapore, International Scientific Committee Member, April 12–15, 2005.
15. EC'2005 (*The 2nd International Workshop on Embedded Computing*), Oslo, Norway, June 14–17, 2005.
16. PDES'2005 (*The 1st International Workshop on Parallel and Distributed Embedded Systems*), Fukuoka Institute of Technology, Japan, July 20–22, 2005.
17. CODES+ISSS'2005 (*The 3rd International Symposium on Hardware-Software Codesign and System Synthesis*), New York, USA, September 19-21, 2005.
18. ATVA'2005 (*The 3rd International Symposium on Automated Technology for Verification and Analysis*), National Taiwan University, Taipei, Taiwan, October 2005.
19. TFIT'2005 (*The 2nd Taiwanese-French Conference in Information Technologies*), National Cheng Kung University, Tainan, Taiwan, March 2005.
20. HPC'2005 (*The 2005 International Conference on High Performance Computing and Communications*), Sorrento (Naples), Italy, September 2005.
21. EUC'2005 (*The 2005 IFIP International Conference on Embedded and Ubiquitous Computing*), Nagasaki, Japan, December 2005.
22. AINA'2006 (*The 20th IEEE Advanced Information Networking and Applications*), Vienna, Austria, April 2006.
23. EC'2006 (*The 3rd International Workshop on Embedded Computing*), Columbus, Ohio, USA, August 2006.
24. ESO'2006 (*The 1st International Workshop on Embedded Software Optimization*), Soeul, Korea, August 2006.
25. IWSE'2006 (*The 2006 International Workshop on Software Engineering*, Hong Kong, China, June 2006. (in conjunction with IMECS'2006)
26. EUC'2006 (*The 2006 IFIP International Conference on Embedded and Ubiquitous Computing*), Soeul, Korea, August 2006.
27. CODES+ISSS'2006 (*The 4th International Symposium on Hardware-Software Codesign and System Synthesis*), Seoul, Korea, October 23-25, 2006.
28. RTCSA'2006 (*The 12th IEEE International Conference on Embedded and Real-Time Computing and Applications*), Sidney, Australia, August 16-18, 2006.

29. SAPC'2006 (*The 1st International Workshop on Software and Algorithmic Aspects of Pervasive Computing*), Changsha, China, October 21-23, 2006.
30. SoC'2006 (*International Workshop on SoC and MCSoc Design*, in conjunction with the 4th International Conference on Advances in Mobile Computing and Multimedia), Yogyakarta, Indonesia, December 4-6, 2006.
31. ICMUE'2007 (*The International Conference on Multimedia and Ubiquitous Engineering*), Cheju Island, Korea, November 9-11, 2007.
32. IRMA'2007 (*The Information Resources Management Association International Conference*), Vancouver, Canada, May 19-23, 2007.
33. ICSE'2007 (*IAENG International Conference on Software Engineering*), Hong Kong, March 21-23, 2007.
34. MCSoc'2007 (*International Workshop on Embedded Single and Multicore Systems on Chips*), XiAn, China, September 10-14, 2007.
35. ICESS'2007 (*International Conference on Embedded Software and Systems*), Korea, May 14-16, 2007.
36. SPAC'2007 (*The First IEEE International Workshop on Software Patterns: Addressing Challenges*), Beijing, China, July 24-27, 2007.
37. CODES+ISSS'2007 (*The 5th International Symposium on Hardware-Software Codesign and System Synthesis*), Salzburg, Austria, September 30-October 5, 2007.
38. IPC'2007 (*The 2007 International Conference on Intelligent Pervasive Computing*), Jeju Island, Korea, October 12-13, 2007.
39. USE'2007 (*The 1st IEEE/ACM International Workshop on Unified Software Engines for Any Domain: Addressing The Challenges*, Atlanta, Georgia, November 5-9, 2007.
40. IHS'2007 (*International Workshop on Intelligent Healthcare Systems*), in conjunction with IPC'2007 (*Intelligent Pervasive Computing*), Jeju Island, Korea, October 2007.
41. NCS'2007 (*National Computer Symposium*), Taichung Taiwan, December 2007.
42. ICMUE'2008 (*The International Conference on Multimedia and Ubiquitous Engineering*), Soeul, Korea, April 2008.
43. ISA'2008 (*The International Conference on Information Security and Assurance*), Busan, Korea, April 2008.
44. ICESS'2008 (*The 2008 International Conference on Embedded Software and Systems*), Sichuan, China, July 2008.
45. DIPES'2008 (*IFIP Working Conference on Distributed and Parallel Embedded Systems*), Milano, Italy, September 2008.
46. SEC'2008 (*5th IEEE International Symposium on Embedded Computing*), Beijing, China, October 2008.
47. TCSE'2008 (*4th Taiwan Conference on Software Engineering*), Tainan, Taiwan, June 2008.

48. CODES+ISSS'2008 (*The 5th International Symposium on Hardware-Software Codesign and System Synthesis*), Atlanta, Georgia, October 19-24, 2008.
49. EUC'2008 (*The 2008 IFIP International Conference on Embedded and Ubiquitous Computing*), Shanghai, China, December 17-20, 2008.
50. ESO'2008 (*The 3rd International Workshop on Embedded Software Optimization*), Shanghai, China, December 17-20, 2008.
51. PAL'2008 (*Conference on Innovative Application of System Prototyping and Circuit Design*), PAL Forum, Ministry of Education, National Chin-Yi University of Technology, Taiwan, October 2008.
52. ICESS'2009 (*The 2009 International Conference on Embedded Software and Systems*), Zhejiangan, China, May 2009.
53. MCSoc'2009 (*The 4th International Symposium on Embedded Multicore Systems-on-Chip*), Vienna, Austria, September 2009.
54. ISPAN'2009 (*The International Symposium on Pervasive Systems, Algorithms, and Networks*), Kaohsiung, Taiwan, December 2009.
55. CODES+ISSS'2009 (*The 6th International Conference on Hardware-Software Codesign and System Synthesis*), Grenoble, France, October 11-16, 2009.
56. EUC'2009 (*The 2009 IFIP International Conference on Embedded and Ubiquitous Computing*), Vancouver, Canada, August 29-31, 2009.
57. TCSE'2009 (*4th Taiwan Conference on Software Engineering*), Tainan, Taiwan, June 2009.
58. ICFPT'2009 (*The 2009 International Conference on Field-Programmable Technology*), Sydney, Australia, December 9–11, 2009.
59. EM-Com'2009 (*The 4th International Conference on Embedded and Multimedia Computing*), Jeju, Korea, December 10–12, 2009.
60. NCS'2009 (*National Computer Symposium*), Taiwan, December 2009.
61. MulGraB'2009 (*The 1st International Conference on Multimedia, Computer Graphics and Broadcasting*), Jeju Island, Korea, December 2009.
62. FPGA'2009 (*Workshop on Innovations and Applications in System Prototyping and Circuit Design*), Taiwan, October 16, 2009.
63. ITNG'2010 (*1st International Symposium on Networking and Wireless Communications*), Las Vegas, USA, April 12–14, 2010.
64. PDP'2010 (*The 18th Euromicro International Conference on Parallel, Distributed and Network-Based Computing*), Special session on On-Chip Parallel and Network-Based Systems, Pisa, Italy, February 17–19, 2010.
65. DIPES'2010 (*IFIP Working Conference on Distributed and Parallel Embedded Systems*), Brisbane, Australia, September 2010.
66. UCMA'2010 (*The 2010 International Conference Ubiquitous Computing and Multimedia Applications*), India, June 3–5, 2010.
67. UME'2010, 2010.

68. MulGraB'2010 (*The 2nd International Conference on Multimedia, Computer Graphics and Broadcasting*), Cebu Philipines, November 2010.
69. MCSoC'2010 (*The 5th International Symposium on Embedded Multicore Systems-on-Chip*), San Diego, California, USA, September 2010.
70. FPL'2010, (*The 20th International Conference on Field Programmable Logic and Applications*), Milano, Italy, August 31-September 2, 2010.
71. ICESSE'2010, (*The 7th IEEE International Conference on Embedded Software and Systems*), Bradford, UK, 29 June - 1 July, 2010.
72. CODES+ISSS'2010 (*The International Conference on Hardware-Software Code-sign and System Synthesis*), Scottsdale, Arizona, USA, on October 24-29, 2010.
73. OOTA+TCSE'2010, (*2010 Joint Conference on Object-Oriented Technology and Applications (OOTA) and Software Engineering (TCSE)*), Taiwan, July 2010.
74. ReConFig'2010, (*2010 International Conference on Reconfigurable Computing and FPGAs*), Cancun, Mexico, December 6–8, 2010.
75. FPT'2010 (*The 2010 International Conference on Field-Programmable Technology*), Beijing, China, December 8–10, 2010.
76. CUTE'2010 (*The 5th International Conference on Ubiquitous Information TEchnologies & Applications*), Sanya, China, December 2010.
77. UMCC'2010 (*The First International Workshop on Ubiquitous Multimedia Computing and Communication*), Xi'an, China, October 2010.
78. ITNG'2011 (*2nd International Symposium on Networking and Wireless Communications*), Las Vegas, USA, April 11–13, 2011.
79. CODES+ISSS'2011 (*The International Conference on Hardware-Software Code-sign and System Synthesis*), Taipei, Taiwan, on October 9-14, 2011.
80. UCMA'2011 (*The 2nd International Conference Ubiquitous Computing and Multimedia Applications*), Korea, April 13–15, 2011.
81. FPL'2011 *The 21st International Conference on Field Programmable Logic and Applications*, Chania, Greece, September 5-7, 2011.
82. ICPP-EMS'2011 *The 2011 International Workshop on Embedded Multicore Systems*, Taipei, Taiwan, September 13-16, 2011.
83. ATVA'2011 (*The 9th International Symposium on Automated Technology for Verification and Analysis*), Taipei, Taiwan, October 2011.
84. ERSA'2011 (*The International Conference on Engineering of Reconfigurable Systems and Algorithms*), Las Vegas, USA, July 18-22, 2011.
85. GreenCom'2011 (*The 2011 IEEE/ACM International Conference on Green Computing and Communications*), Chengdu, Sichuan, China, August 4-5, 2011.
86. ReConFig'2011, (*2011 International Conference on Reconfigurable Computing and FPGAs*), Cancun, Mexico, December 6–8, 2011.
87. EUC'2011 (*The 9th IEEE/IFIP International Conference on Embedded and Ubiquitous Computing*), Melbourne, Australia, October 24–26, 2011.

88. TCSE-OOTA'2011 (*2011 Joint Conference on Taiwan Software Engineering (TCSE) and Object-Oriented Technology and Applications (OOTA)*), Taiwan, July 8–9, 2011.
89. ICESSE'2011 (*8th IEEE International Conference on Embedded Software and Systems*), Chang-Sha, China, November 16-18, 2011.
90. ESA'2011 (*2nd IEEE International Symposium on Advanced Topics on Embedded Systems and Applications*), Chang-Sha, China, November 16-18, 2011.
91. EmbeddedCom'2011 (*The 9th International Symposium on Embedded Computing*), Sydney, Australia, December 12-14, 2011.
92. ASP-DAC 2012 (*17th Asia and South Pacific Design Automation Conference*), Sydney, Australia, January 30 - February 2, 2012.
93. VLSI-DAT 2012 (*International Symposium on VLSI Design, Automation and Test*), Taiwan, April 2012.
94. MCSoC 2012 (*IEEE International Symposium on Embedded Multicore System-on-Chip*), Aizu-Wakamatsy, Japan, September 20-22, 2012.
95. EMC 2012 (*7th International Conference on Embedded and Multimedia Computing*), Korea, September 6–8, 2012.
96. GreenCom'2012 (*The 2012 IEEE/ACM International Conference on Green Computing and Communications*), Besancon, France, September 11-14, 2012.
97. FPL'2012 (*The 22nd International Conference on Field Programmable Logic and Applications*), Oslo, Norway, August 29-31, 2012.
98. ReCoSoC'2012 (*7th International Workshop on Reconfigurable Communication-Centric Systems-on-Chip*), York, UK, July 9-11, 2012.
99. CODES+ISSS'2012 (*The International Conference on Hardware-Software Code-design and System Synthesis*), Tampere, Finland, on October 7-12, 2012.
100. ICPP-EMS'2012 (*The 2012 International Workshop on Embedded Multicore Systems*), Pittsburgh, USA, September 10-13, 2012.
101. EUC'2012 (*The 10th IEEE/IFIP International Conference on Embedded and Ubiquitous Computing*), October 2012.
102. TCSE'2012 (*2012 Taiwan Conference on Software Engineering (TCSE)*), Taiwan, July 6–7, 2012.
103. ICS'2012 (*International Computer Symposium*), Workshop on Software Engineering and Programming Languages, 2012.
104. ReConFig'2012, (*2012 International Conference on Reconfigurable Computing and FPGAs*), Cancun, Mexico, December 5–7, 2012.
105. APSEC'2012 (*The 19th Asia-Pacific Software Engineering Conference*), Emerging Research Track, Hong-Kong, December 4-7, 2012.
106. SmartIT'2012 (*International Workshop on Smart Devices, Applications, and Services*), Jeju, Korea, November 22-25, 2012.
107. WorldCIST'2013 (*The 2013 World Conference on Information Systems and Technologies*), Olhão, Algarve, Portugal , March 27-30, 2013.

108. VLSI-DAT'2013 (*International Symposium on VLSI Design, Automation and Test*, April 22-24, 2013).
109. ACCESS'2013 (The International Congress on Advances in Citizen, Cyberspace & Environment Safety and Security), Singapore, 5–7 June 2013.
110. RAW'2013 (*The 20th Reconfigurable Architecture Workshop*), Boston, USA, May 20-21, 2013.
111. MCSoc'2013 (*IEEE 7th International Symposium on Embedded Multicore SoCs*), Tokyo, Japan, September 26-28, 2013.
112. ICPP-EMS'2013 *The 2013 International Workshop on Embedded Multicore Systems*, Lyon, France, October 1-4, 2013.
113. UCMA'2013 (*The 4th International Conference on Ubiquitous Computing and Multimedia Applications*), Xian China, May 23-25, 2013.
114. ePaMuS'2013(*The 6th International Workshop on Engineering Parallel and Multi-Core Systems*), Taichung, Taiwan, July 3-5, 2013.
115. NBiS'2013 (*16th International Conference on Network-Based Information Systems*), Gwangju, Korea, September 4-6, 2013.
116. FPL'2013 (*23rd International Conference on Field Programmable Logic and Applications*), Porto, Portugal, September 2-4, 2013.
117. CODES+ISSS'2013 (*The International Conference on Hardware-Software Code-sign and System Synthesis*), Montreal, Canada, on September 29-October 4, 2013.
118. INTERNET'2013 (*The 5th International Conference on Evolving Internet*), Nice, France, July 21-26, 2013.
119. GreenCom'2013 (*IEEE International Conference on Green Computing and Communications*), Beijing, China, August 20-23, 2013.
120. ReCoSoC'2013 (*8th International Workshop on Reconfigurable Communication-Centric Systems-on-Chip*), Darmstadt, Germany, July 10-12, 2013.
121. EMC 2013 (*8th International Conference on Embedded and Multimedia Computing*), Taipei, Taiwan, August 22–24, 2013.
122. EITA 2013 (*Computers, Communications and IT Applications Conference*), Hong Kong, April 1-4, 2013.
123. SQHE 2013 (*International Workshop on Software Quality Assurance of Healthcare System and Embedded System*), Nanjing, China, July 29-30, 2013.
124. EUC'2013 (*The 11th IEEE/IFIP International Conference on Embedded and Ubiquitous Computing*), Zhangjiajie, China, November 2013.
125. TCSE'2013 (*2013 Taiwan Conference on Software Engineering (TCSE)*), Taiwan, July 5–6, 2013.
126. ICESS'2013 (*The 10th IEEE International Conference on Embedded Software and Systems*), Sydney, Australia, December 3-5, 2013.
127. ReConFig'2013, (*2013 International Conference on Reconfigurable Computing and FPGAs*), Cancun, Mexico, December 9-11, 2013.

128. APHC'2013 (*12th Asia-Pacific HL7 Conference on Health Care Information Standards*), Taipei, Taiwan, October 25-26, 2013.
129. NCS'2013 (*National Computer Symposium*), Workshop on Programming Language and Software Engineering, Taichung, December 13-14, 2013.
130. CECNet'2013 (*3rd International Conference on Consumer Electronics, Communications, and Networks*), Shenzhen, China, November 2013.
131. ICITCS'2013, (*International Conference on IT Convergence and Security*), Macau, China, December 16-18, 2013 .
132. HP3C'2014 (*International Conference on High Performance Compilation, Computing and Communications*), Aizu, Japan, September 24-26, 2014.
133. RAW'2014 (*The 21st Reconfigurable Architecture Workshop*), Phoenix, USA, May 18-19, 2014.
134. WRC'2014 (*8th HiPEAC Workshop on Reconfigurable Computing*), Vienna, Austria, January, 2014.
135. INTERNET'2014 (*The 6th International Conference on Evolving Internet*), Seville, Spain, June 22-26, 2014.
136. CISIS'2014 (*The 8th International Conference on Complex, Intelligent, and Software Intensive Systems*), Birmingham, UK, July 2-4, 2014.
137. ICPP-EMS'2014 *The 2014 International Workshop on Embedded Multicore Systems*, USA, September 9-12, 2014.
138. COMPSAC'2014 (*38th IEEE International Computer Software and Applications Conference*), Västerås, Sweden, July 21-25 2014.
139. TSA'2014 (*1st International Conference on Trustworthy Systems and Applications*), Taichung, Taiwan, May 29-30, 2014.
140. FPL'2014 (*24th International Conference on Field Programmable Logic and Applications*), Munich, Germany, September 2-4, 2014.
141. EUC'2014 (*The 12th IEEE/IFIP International Conference on Embedded and Ubiquitous Computing*), Milan, Italy, August 2014.
142. ICCESS'2014, (*11th IEEE International Conference on Embedded Software and Systems*), Paris, France, August 20-22, 2014.
143. EmbeddedCom'2014, (*12th IEEE International Conference on Embedded Computing*), Dalian, China, August 24-27, 2014.
144. SEC'2014 (*The International Conference on Smart Electronics and Communication*), Dalian, China, August 18-20, 2014.
145. EMC'2014 (*The 9th International Conference on Embedded and Multimedia Computing*), Ostrava, Czech Republic, August 25-17, 2014.
146. TCSE'2014 (*2014 Taiwan Conference on Software Engineering (TCSE)*), Taiwan, June 29-30, 2014.
147. VLSI Design'2014 (*The 25th VLSI Design/CAD Symposium*), Taichung, August 5-8, 2014.

148. CODES+ISSS'2014 (*The International Conference on Hardware-Software Code-sign and System Synthesis*), New Delhi, India, October 2014.
149. DASC'2014 (*12th IEEE International Conference on Dependable, Autonomic and Secure Computing*), Dalian, China, August 24–27, 2014.
150. ICS'2014 (*International Computer Symposium*), Taichung, Taiwan, December 2014.
151. INNOV'2014 (*The Third International Conference on Communications, Computation, Networks and Technologies*), Nice, France, October 12–16, 2014.
152. DEPEND'2014 (*The Seventh International Conference on Dependability*), Lisbon, Portugal, November 16-20, 2014.
153. ReConFig'2014, (*2014 International Conference on Reconfigurable Computing and FPGAs*), Cancun, Mexico, December 8-10, 2014.
154. MulGraB'2014 (*The 6th International Conference on Multimedia, Computer Graphics and Broadcasting*), Hainan, China, December 2014.
155. INTERNET'2015 (*The 7th International Conference on Evolving Internet*), St. Julians, Malta, October 11-16, 2015.
156. ATVA'2015 (*The 13th International Symposium on Automated Technology for Verification and Analysis*), Shanghai, China, October 2015.
157. WRC'2015 (*9th HiPEAC Workshop on Reconfigurable Computing*), January 20, 2015, Amsterdam, The Netherlands.
158. CLOUD COMPUTING'2015 (*The 6th International Conference on Cloud Computing, GRIDs, and Virtualization*), Nice, France, March 2015.
159. iWAPT'2015 (*The Tenth International Workshop on Automatic Performance Tuning*), India, May 2015.
160. EMERGING'2015 (*The Seventh International Conference on Emerging Network Intelligence*), Nice, France, July 2015.
161. INNOV'2015 (*The Fourth International Conference on Communications, Computation, Networks and Technologies*), Spain, November 2015.
162. DEPEND'2015 (*The Eighth International Conference on Dependability*), Venice, Italy, August 23-28, 2015.
163. CODES+ISSS'2015 (*The International Conference on Hardware-Software Code-sign and System Synthesis*), Amsterdam, The Netherlands, October 2015.
164. ICITCS'2015 (*The 5th International Conference on IT Convergence and Security*), Kuala Lumpur, Malaysia, August 2015.
165. ReConFig'2015, (*2015 International Conference on Reconfigurable Computing and FPGAs*), Mayan Riviera, Mexico, December 7-9, 2015.
166. PICom'2015, (*The 13th IEEE International Conference on Pervasive Intelligence and Computing*), Liverpool, UK, October 2015.
167. GLOBAL TIE SUMMIT'2016 (*6th International Conference on Cloud System and Big Data Engineering*), UP, India, January 2016.

168. CLOUD COMPUTING'2016 (*The 7th International Conference on Cloud Computing, GRIDs, and Virtualization*), Rome, Italy, March 2016.
169. WRC'2016 (*10th HiPEAC Workshop on Reconfigurable Computing*), Amsterdam, The Netherlands, January 19, 2016.
170. ICC'2016 (*International Conference on Internet of Things and Cloud Computing*), Cambridge, UK, March 22-23, 2016.
171. PICom'2016, (*The 14th IEEE International Conference on Pervasive Intelligence and Computing*), Auckland, New Zealand, August 2016.
172. EMERGING'2016 (*The Eighth International Conference on Emerging Networks and Systems Intelligence*), Venice, October 2016.
173. DEPEND'2016 (*The Ninth International Conference on Dependability*), Nice, France, July 24-28, 2016.
174. ICMWT'2016 (*International Conference on Mobile and Wireless Technology*), Jeju, Korea, May 26, 2016.
175. INTERNET'2016 (*The 8th International Conference on Evolving Internet*), Barcelona, Spain, November 13-17, 2016.
176. PEC'2106 (*International Conference on Pervasive and Embedded Computing*), Lisbon, Portugal, July 25–27, 2016.
177. BICTA'2016 (*2nd International Conference on Big-data, IoT, Cloud Computing Technologies and Applications*), Jeju, Korea, March 24–26, 2016.
178. CODES+ISSS'2016 (*The International Conference on Hardware-Software Code-design and System Synthesis*), Pittsburgh, USA, October 2–7, 2016.
179. INNOV'2016 (*The Fifth International Conference on Communications, Computation, Networks and Technologies*), Brussels, Belgium, August 21–25, 2016.
180. VLSI Design/CAD Symposium (*The 27th VLSI Design/CAD Symposium*), Hualien, Taiwan, August 4–7, 2016.
181. InCITe'2016 (*International Conference on Information Technology*), 2016.
182. TCSE'2016 (*2016 Taiwan Conference on Software Engineering*), Taiwan, July 8–9, 2016.
183. Internetware'2016 (*The Eighth Asia-Pacific Symposium on Internetware*), Beijing, China, September 18, 2016.
184. ReConFig'2016, (*2016 International Conference on Reconfigurable Computing and FPGAs*), Cancun, Mexico, December 2, 2016.
185. TSA'2016 (*IEEE International Conference on Trustworthy Systems and Applications*), Wuhan, China, September 18-20, 2016.
186. ICCE'2017 (*International Conference on Consumer Electronics*), Las Vegas, USA, January 2017.
187. PEC'2107 (*International Conference on Pervasive and Embedded Computing*), Madrid, Spain, July 27–29, 2017.
188. WRC'2017 (*11th HiPEAC Workshop on Reconfigurable Computing*), Stockholm, Sweden, January 23, 2017.

189. ICATE'2017 (*International Conference on Advanced Technologies Enhancing Education*) Qingdao, China, March 18–20, 2017.
190. CSICT'2017 (*International Conference on Computer Science and Information Communication*), Qingdao, China, March 18–20, 2017.
191. PICom'2017, (*The 15th IEEE International Conference on Pervasive Intelligence and Computing*), Orlando, Florida, November 2017.
192. INTERNET'2017 (*The 9th International Conference on Evolving Internet*), Nice, France, July 23-27, 2017.
193. ICIT'2017 (*International Conference on Intelligent Information Technology*), Chennai, India, December 20-22, 2017.
194. TCSE'2017 (*2017 Taiwan Conference on Software Engineering (TCSE)*), Taiwan, July 7-8, 2017.
195. DEPEND'2017 (*The Tenth International Conference on Dependability*), Rome, Italy, September 10–14, 2017.
196. iThings'2017 (*The 10th International Conference on Internet of Things*), Exeter, England, UK, June 21–23, 2017.
197. CEC'2017 (*7th International Conference on Electronics, Communications and Networks*), Hualien, Taiwan, Nov. 24–27, 2017.
198. EMERGING'2017 (*The Ninth International Conference on Emerging Networks and Systems Intelligence*), Barcelona, Spain, November 12–16, 2017.
199. ICITCS'2017 (*7th iCatse Conference on IT Convergence and Security*, South Korea, September 25–28, 2017)
200. ReConFig'2017, (*2017 International Conference on Reconfigurable Computing and FPGAs*), Cancun, Mexico, December 4–6, 2017.
201. NCS'2017, (*National Computer Symposium*), Taiwan, December 2017.
202. SICBS'2017, (*International Conference on Security with Intelligent Computing and Big-data Services*), Taiwan, December 15–17, 2017.
203. NEXTCOM'2017 (*International Conference on Computational Strategies for Next Generation Technologies*), CT Institute of Engineering, Punjab, India, November 25–26, 2017.
204. Confluence'2018 (*The 8th International Conference on Cloud Computing, Data Science and Engineering*), Noida Uttar Pradesh, India, January 11-12, 2018.
205. ESG'2018 (*International Conference on Energy Engineering and Smart Grids*), Oxford, UK, June 4–5, 2018.
206. INTERNET'2018 (*The 10th International Conference on Evolving Internet*), Venice, Italy, June 24-28, 2018.
207. ICSC'2018 (*International Conference on Ingenious Computing and Smart Communication*), Tehri, Uttarakhand, India, March 20–25, 2018.
208. ICRIC'2018 (*International Conference on Recent Innovations in Computing*), J&K, India, March 5–6, 2018.

209. PEC'2018 (*International Conference on Pervasive and Embedded Computing*), Porto, Portugal, July 29–30, 2018.
210. WECON'2018 (*International Conference on Wireless Networks & Embedded Systems*), Chitkara University, India, November 16–17, 2018.
211. MCSoc'2018 (*IEEE 12th International Symposium on Embedded Multicore/Many-core Systems-on-Chips*), Vietnam, September 12-14, 2018.
212. PICom'2018, (*The 16th IEEE International Conference on Pervasive Intelligence and Computing*), Athens, Greece, August 2018.
213. FTNCT'2018, (*Futuristic Trends in Network and Communication Technology*), India, February 2018.
214. SmartCity'2018, (*16th IEEE International Conference on Smart City*), Exeter, England, UK, June 28–30, 2018.
215. ICPP-EMS'2018 *The 2018 International Workshop on Embedded Multicore Systems*, Eugene, Oregon, USA, August 13-16, 2018.
216. TCSE'2018 (*2018 Taiwan Conference on Software Engineering (TCSE)*), Taiwan, July 6-7, 2018.
217. ICCE'2018 (*International Conference on Consumer Electronics*), Las Vegas, USA, January 2018.
218. iThings'2018 (*The 11th International Conference on Internet of Things*), Halifax, Canada, July 30– August 3, 2018.
219. ICAICR'2018 (*2nd International Conference on Advanced Informatics for Computing Research*), Shimla, India, July 14–15, 2018.
220. ReConFig'2018, (*2018 International Conference on Reconfigurable Computing and FPGAs*), Cancun, Mexico, December 3–5, 2018.
221. NCS'2018, (*10th International Conference on Network and Communications Security*), Dubai, UAE, December 22–23, 2018.
222. PDGC'2018 (*Fifth IEEE International Conference on Parallel and Distributed Computing*), 2018.
223. ICCE'2019 (*International Conference on Consumer Electronics*), Las Vegas, USA, January 2019.
224. ASPAI'2019 (*The 1st International Conference on Advances in Signal Processing and Artificial Intelligence*), Barcelona, Spain, March 20–22, 2019.
225. CONFLUENCE'2019 (*9th International Conference on Cloud Computing, Data Science and Engineering*), January 10–11, 2019.
226. ICS'2019 (*International Computer Symposium*), Yunlin, Taiwan, December 2019.

16 Conference Organization and Chairing

Dr. Hsiung has been actively seeking to organize conference sessions and international workshops in his fields of research interests.

1. **Session Organizer/Program Chair**, PDPTA'99 (*International Conference on Parallel and Distributed Processing Techniques and Applications*), *Special Session on Hardware-Software Codesign of Parallel and Distributed Systems*, Las Vegas, Nevada, USA, June-July 1999.
2. **Workshop Organizer and Program Chair**, RTC'99 (*International Workshop on Real-Time Constraints*), Alexandria, Virginia, USA, October 1999.
3. **Workshop Organizer and Program Chair**, DSVV'2000 (*International Workshop on Distributed System Validation and Verification*), Taipei, Taiwan, April 2000.
4. **Session Chair**, OOTSIG 2000 (*11th OOTSIG Workshop on Object-Oriented Technology and Applications*), Taichung, Taiwan, September 2000.
5. **Session Chair**, RTCSA 2000 (*7th International Conference on Real-Time Computing Systems and Applications*), Cheju Island, South Korea, December 2000.
6. **Session Chair**, TANET 2001 (*Workshop on Taiwan Academic Network and E-Learning*), Chiayi, Taiwan, November 2001.
7. **Session Chair**, RTCSA 2003 (*9th International Conference on Real-Time Computing Systems and Applications*), Tainan, Taiwan, February 2003.
8. **Program Vice-Chair for HW-SW Codesign and SoC**, EUC'2004 (*International Conference on Embedded and Ubiquitous Computing*), Aizu, Japan, August 26-28, 2004.
9. **Special Track Chair for Hardware-Software Coverification and Cosynthesis**, ATVA'2004 (*International Symposium on Automated Technology for Verification and Analysis*), National Taiwan University, Taipei, Taiwan, October 2004.
10. **Program Co-Chair**, PDES'2005 (*The 1st International Workshop on Parallel and Distributed Embedded Systems*), Fukuoka Institute of Technology, Japan, July 20–22, 2005.
11. **Session Chair**, VLSI Design/CAD'2005 (*VLSI Design / CAD Symposium*), Taiwan, August 2005.
12. **Panel Chair**, EUC'2005 (*The 2005 IFIP International Conference on Embedded and Ubiquitous Computing*), Nagasaki, Japan, December 2005.
13. **Session Chair**, VLSI Design/CAD'2007 (*VLSI Design / CAD Symposium*), Taiwan, August 2007.
14. **Track Co-Chair**, System-Level Design, SOCC 2007 (*IEEE International SoC Conference*), Taiwan, September 2007.
15. **Program Vice-Chair, Track Chair, Panelist** for Embedded Systems and Hardware-Software Co-design, EUC'2009 (*The 2009 IFIP International Conference on Embedded and Ubiquitous Computing*), Vancouver, Canada, August 2009.
16. **Workshop Organizer and Program Chair**, *International Workshop on Reconfigurable and Multicore Embedded Systems (WoRMES)*, August 2009.
17. **Track Chair**, Dynamic Spectrum Access Track, *1st International Symposium on Networking and Wireless Communications*, Las Vegas, USA, April 2010.

18. **Track Chair** for Embedded Systems and Hardware-Software Co-design, EUC'2010 (*The 2010 IFIP International Conference on Embedded and Ubiquitous Computing*), Hong Kong, China SAR, December 2010.
19. **Advisory Committee Member**, *Workshop on FPGA System Prototyping and Circuit Design Innovation*, 2010.
20. **Track Chair**, Dynamic Spectrum Access Track, *2nd International Symposium on Networking and Wireless Communications*, Las Vegas, USA, April 2011.
21. **Program Co-chair**, ATVA'2011 (*The 9th International Symposium on Automated Technology for Verification and Analysis*), Taipei, Taiwan, October 2011.
22. **Conference Co-chair**, ERSA'2011 (*The International Conference on Engineering of Reconfigurable Systems and Algorithms*), Las Vegas, Nevada, USA, July 18-21, 2011.
23. **Publicity Co-Chair**, FPT'2012 (*International Conference on Field-Programmable Technology*), Seoul, Korea, December 2012.
24. **Program Chair**, HMC'2013 (*The 1st International Workshop on Heterogeneous Multi-Core Computing*), Japan, September 2013.
25. **Local Organizing Chair**, ePaMuS'2013 (*The 6th International Workshop on Engineering Parallel and Multi-Core Systems*), Taichung, Taiwan, July 2013.
26. **Steering Committee Member**, MCSoc'2014 (*IEEE 8th International Symposium on Embedded Multicore/Many-core SoCs*), September 2014.
27. **Steering Committee Member**, HP3C'2014 (*International Conference on High Performance Compilation, Computing and Communications*), University of Aizu, Japan, September 2014.
28. **Publicity Chair**, EUC'2014 (*International Conference on Embedded and Ubiquitous Computing*), 2014.
29. **Track Chair**, CISIS'2014 (*The 8th International Conference on Complex, Intelligent, and Software Intensive Systems*), July 2014.
30. **Workshop Chair**, Workshop on Computer Architecture, Embedded Systems, SoC, and VLSI/EDA, International Computer Symposium (ICS), December 2014.
31. **Program Chair**, 39th Annual International Computers, Software & Applications Conference (COMPSAC), Taichung, Taiwan, July 2015.
32. **Publicity Chair**, EUC'2015 (*International Conference on Embedded and Ubiquitous Computing*), 2015.
33. **Program Co-Chair**, ICS'2016 (*International Computer Symposium*), December 2016.
34. **Track Chair**, ICCE'2017 (*International Conference on Consumer Electronics*), Las Vegas, USA, January 2017.
35. **Advisory Committee**, IDEA'2017 (*International Conference on Data Engineering and Applications*), Bhopal, India, October 2017.
36. **Conference Chair**, ICAICR'2017 (*1st International Conference on Advanced Informatics for Computing Research*), India, March 17–18, 2017.

37. **Conference Chair**, NEXTCOM'2017 (*International Conference on Computational Strategies for Next Generation Technologies*), CT Institute of Engineering, Punjab, India, November 25–26, 2017.
38. **Advisory Committee**, TMSI'2018 (*International Conference on Technology, Management and Scientific Innovation towards Skill, Startup and Industrial Growth*), Bhopal, India, February 2018.
39. **Advisory Committee**, PDGC'2018 (*Fifth International Conference on Parallel, Distributed and Grid Computing*), Delhi, India, December 20–22, 2018.
40. **Advisory Committee**, ICSC'2018 (*International Conference on Ingenious Computing and Smart Communication*), Tehri, Uttarakhand, India, March 20–25, 2018.
41. **Program Chair**, CNC-2018 (*1st International Conference on Communication, Networks and Computing*), ITM University, India, March 22–24, 2018.
42. **Conference General Chair**, ICAICR'2018 (*2nd International Conference on Advanced Informatics for Computing Research*), India, July 2018.
43. **Track Chair**, ICCE'2018 (*International Conference on Consumer Electronics*), Las Vegas, USA, January 2018.
44. **Track Chair**, NICS'2018 (*The 5th NAFOSTED Conference on Information and Computer Science*), Ho Chi Minh City, Vietnam, November 23–24, 2018.
45. **Track Chair**, ICCE'2019 (*International Conference on Consumer Electronics*), Las Vegas, USA, January 2019.

17 Students Advised

17.1 Doctoral Students

1. See, Win-Bin, Ph.D., National Taiwan University, Department of Electrical Engineering, July 2003. (co-advised with Prof. Sao-Jie Chen)
2. Lin, Shang-Wei, Ph.D., “Counterexample-Guided Assume-Guarantee Synthesis Through Learning,” National Chung Cheng University, Department of Computer Science and Information Engineering, July 2010.
3. Huang, Chun-Hsian, Ph.D. “Model-Based Platform-Specific Co-Design Methodology for Dynamically Partially Reconfigurable Systems with Hardware Virtualization and Preemption,” National Chung Cheng University, Department of Computer Science and Information Engineering, January 2011.
4. Shen, Jih-Sheng, Ph.D., “Learning-based Reconfiguration of Network-on-Chip for Varying Processing Requirements,” National Chung Cheng University, Department of Computer Science and Information Engineering, July 2013.
5. Shih, Kai-Jung, Ph.D., “Application Acceleration Using Dynamically Partially Reconfigurable System Infrastructure,” National Chung Cheng University, Department of Computer Science and Information Engineering, July 2013.

6. Lin, Chao-Sheng, Ph.D., “Model-Driven Framework for Multicore Software Development,” National Chung Cheng University, Department of Computer Science and Information Engineering, July 2014.
7. Lin, Chih-Sheng, Ph.D., “Application Synthesis and Optimization on Heterogeneous Parallel Processing Systems,” National Chung Cheng University, Department of Computer Science and Information Engineering, July 2014.
8. Chao, Hung-Lin, Ph.D., “Model-Predictive Optimization for Smart Grid Design,” National Chung Cheng University, Department of Computer Science and Information Engineering, July 2016.
9. Lu, Chun-Hsien, Ph.D. “Landslide Prediction – A Cyber-Physical System Design,” National Chung Cheng University, Department of Computer Science and Information Engineering, July 2016.
10. Huang, Ken-Shin, Ph.D. “Adaptive Reasoning and Learning Framework for Cognitive Radio,” National Chung Cheng University, Department of Computer Science and Information Engineering, July 2017.

17.2 Master Students

(Theses available: http://embedded.cs.ccu.edu.tw/~esl_web/Ch/masterPaper.php)

1. Su, Feng-Shi, “Formal Synthesis and Code Generation of Embedded Software Using Extended Quasi-Static Scheduling,” National Chung Cheng University, Department of Computer Science and Information Engineering, June 2002. (**Merit Award from IICM, 2002**)
2. Gau, Chuen-Hau, “Time-Memory Scheduling and Code Generation for Real-Time Embedded Software,” National Chung Cheng University, Department of Computer Science and Information Engineering, June 2002.
3. Jeng, Shu-Yu, “Automating Assume-Guarantee Reasoning for Model Checking Real-Time Embedded Systems,” National Chung Cheng University, Department of Computer Science and Information Engineering, June 2002.
4. Shen, Tzu-Yung, “Assume-Guarantee Formal Verification of Component-Based Hierarchical Software,” National Chung Cheng University, Department of Computer Science and Information Engineering, July 2003.
5. Lin, Cheng-Yi, “Quasi-Dynamic Scheduling for the Formal Synthesis of Real-Time Embedded Software,” National Chung Cheng University, Department of Computer Science and Information Engineering, July 2003. (**Merit Award from IICM, 2003**)
6. Chen, Li-Ming, “Interface Synthesis of Real-Time Embedded Systems,” National Chung Cheng University, Department of Computer Science and Information Engineering, July 2003.
7. Sun, Ming-Huang, “Formal Specification Generation by Applying Error Trace Analysis for Semi-Formal Verification,” National Chung Cheng University, Department of Computer Science and Information Engineering, July 2003.

8. Chang, Yu-Ming, "CORBA-based Distributed Formal Verification," National Chung Cheng University, Department of Computer Science and Information Engineering, January 2004.
9. Liao, Wen-Shiu, "Infrastructure of a Formal Verification Platform for SoC," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2004. (**Merit Award from IICM, 2004**)
10. Kao, Hsin-Chieh, "Device-Centric Energy-Optimal Scheduling for Low-Power Real-Time Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2004.
11. Li, Te-Chang, "Mutation Coverage Estimation for Symbolic Model Checking," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2004.
12. Wu, Chan-Chi, "An Assertion-based Dynamic Formal Verification Methodology for Hardware Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2004.
13. Chao, Wei-Cheng, "Transaction-Level Modeling for Modeling Checking," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2004.
14. Tsai, Wei-Yu, "Formal Verification of Safety-Critical Systems with Safecharts," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2004.
15. Chiu, Kuan-Lun, "An Efficient Coverage Estimation Methodology for Model Checking," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2005.
16. Chen, Yuan-Hsiu, "Hardware Scheduling and Placement in Operating Systems for Reconfigurable SoC," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2005.
17. Liao, Chih-Feng, "A SystemC Based Performance Evaluation Framework for Dynamically Reconfigurable SoC," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2005.
18. Tseng, Chih-Hao, "UML-Based Rapid Prototyping Design Flow for Dynamically Reconfigurable Computing Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2005. (**Merit Award from IICM, 2005**)
19. Wang, Hung-Ren, "Hardware-Software Codesign for Programmable SoC," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2005.
20. Yeh, Jia-Jen, "An Efficient Coverage Estimation Methodology for Model Checking," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2006.

21. Chen, Yean-Ru, "Automatic Failure Analysis using Extended Safecharts," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2006. (**Merit Award from IICM, 2006**)
22. Liu, Chih-Wen, "Energy Efficient Hardware/Software Co-scheduling in Reconfigurable Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2006.
23. Chang, Shih-Hsueh, "Hardware/Software Communication in the Dynamically Partially Reconfigurable Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2006.
24. Lu, Pin-Hsian, "Dynamically Switching Between Hardware Abstraction Models for Rapid Embedded Software Development," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2006.
25. Hsu, Shu-Yu, "Integration of Household Network Gateway and Remote Monitor System based on Embedded System," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2006.
26. Lin, Chao-Sheng, "IP-based Resource Management in Reconfigurable Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2007.
27. Liao, Hsiao-Win, "Multi-Objective Placement of Reconfigurable Hardware Tasks in Real-Time Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2007. (**Merit Award from IICM, 2007**)
28. Chiang, Cheng-Chi, "Hardware/Software Real-Time Relocatable Task Scheduling and Placement in Dynamically Partial Reconfigurable Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2007.
29. Hung, Chin-Chieh, "Reconfigurable Hardware Module Sequencer for Dynamically Partially Reconfigurable Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2007.
30. Sun, Hong-Yu, "Dynamic Hardware-Software Task Switching and Relocation for Reconfigurable Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2007.
31. Chiang, Kuo-Cheng, "Predictable and Adaptive Reconfigurable Network-on-Chip," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2008. (**Merit Award from IICM, 2008**)
32. Tsao, Chih-Chieh, "An Efficient Collaborative Verification Methodology for Multiprocessor SoC with Run-Time Task Migration," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2008.
33. Lin, Yi-Hsun, "Quality-of-Service Optimization for Multiple Multimedia Tasks in Real-Time Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2008.

34. Chiu, Jying-Lwen, "On-line Scheduling of Real-Time Tasks and Compact Placement Method for Dynamically Partially Reconfigurable System," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2008.
35. Lin, Wei-Wen, "An Efficient Hardware/Software Communication Mechanism for Reconfigurable Network-on-Chip," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2009. (**Merit Award from IICM, 2009**)
36. Lan, Chun-Ting, "Dynamic Hardware-Software Task Migration and Relocation Coordinator for Partially Reconfigurable Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2009.
37. Pan, Shen-Yang, "Dynamically Adaptive Arbitration in Network-on-Chip for Streaming Applications," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2010.
38. Lu, Shih-Shen, "Congestion- and Energy-aware Run-time Task Mapping for Network-on-Chip Architecture," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2010. (**Merit Award from IICM, 2010**)
39. Su, Wan-Ting, "Buffer-Stealing Router Design for Improved Communication Efficiency in Network-on-Chip," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2010.
40. Tung, Sheng-Ya, "Dynamic Task Scheduling with Congestion Speculation for Network-on-Chip," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2010.
41. Chen, Li-Chi, "Power Monitoring and Demand Control System Research and Design," National Chung Cheng University, Department of Communication Engineering, January 2011.
42. Chang, Yi-Luen, "An Efficient and Robust Solver for Multi-Objective Constraints-Satisfaction Problem in Cognitive Radio Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, July 2011.
43. Ho, Chia-Chiao, "Dynamic Application Scheduling on Heterogeneous Multi-core Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, July 2011.
44. Lin, Yu-Shin, "Multi-Objective Exploitation of Pipeline Parallelism using Clustering, Replication, and Duplication in Embedded Multicore Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, July 2011.
45. Wang, Bo-Hsuan, "Synchronization-Aware Dynamic Thread Scheduling for Improving Performance and Saving Energy in Multi-Core Embedded Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, July 2011.
46. Shiu, Huei-Min, "RFID-based Roll-Call System for School Campus," National Chung Cheng University, Department of Communication Engineering, July 2011.

47. Shih, Chun-Yi, "Communication Bottleneck Analysis for Improving the Performance of Multicore Software," National Chung Cheng University, Department of Computer Science and Information Engineering, July 2012.
48. Hu, Ya-Ping, "Robust Solution Space Prediction and Optimization for Cognitive Radios," National Chung Cheng University, Department of Computer Science and Information Engineering, July 2012.
49. Wu, Chia-En, "A Study on the Critical Success Factors of Initiating Information Security Management System: Take a University in Northern Taiwan as a Sample," National Chung Cheng University, Department of Communication Engineering, July 2012.
50. Chang, Chun-Chin, "The Research of Radio Frequency Identification Technology for the Family Violence Prevention," National Chung Cheng University, Department of Communication Engineering, July 2012.
51. Chen, Ying-Yu, "RFID-based Roll-Call System Study for Field Trips," National Chung Cheng University, Department of Communication Engineering, January 2013.
52. Yu, Ming-Yu, "Hidden Markov Model-based Bandwidth Selection for Cognitive Network," National Chung Cheng University, Department of Communication Engineering, January 2013.
53. Ko, Yung-Ming, "UHF Bi-directional Tracking System Design by Integrating GPS and Radar Transponder," National Chung Cheng University, Department of Communication Engineering, June 2013.
54. Liao, Wei-Chih, "A Study on the Use of Miracast Supported Devices for Distance Learning," National Chung Cheng University, Department of Communication Engineering, June 2013.
55. Wu, Cheng-Chien, "FPGA-based High Applicability Reconfigurable FFT Processor for Multi-standard Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2013.
56. Perng, Jun-Yang, "Spatio-Temporally-Shared Reconfigurable Fast Fourier Transform Architecture Design," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2013.
57. Teng, Shih-Meng, "Auto-tuning on GPGPU by using Performance and Power Estimation Model," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2013.
58. Chen, Yen-Ting, "Workload Partitioning and Scheduling on Heterogeneous Multi-Core Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2013.
59. Kuo, Hui-Min, "Zigbee-based Roadside Parking System," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2014.
60. Wu, Wen-Yi, "Using Smart Meters for Home Energy Saving," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2014.

61. Yao, Jui-Lung, "SAT-based Verification of Role-based Access Control Systems with Slicing method," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2014.
62. Liu, Po-Ting, "Feedback Control Optimization for Performance and Energy Efficiency on CPU-GPU Heterogeneous Systems," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2014.
63. Soong, Yi-Chien, "Interference-aware Batch Memory Scheduling in Heterogeneous Multi-core Architecture," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2014.
64. Wang, Jien-Yu, "Elastic Superposition Mapping for Heterogeneous Tasks in Reconfigurable Multicore Architecture," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2014.
65. Tsai, Chen-Chou, "Hierarchical Optimization of Smart Grids with Energy Storage Systems - A Model-Predictive Control and Auction-based Method," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2014.
66. Liu, Yan-Dun, "Smart Photovoltaic Power Generation System Design," National Chung Cheng University, Department of Computer Science and Information Engineering, January 2014.
67. Wu, Tsung-Tien, "Software-Defined Network Interface Design Performance and Security Oriented," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2015.
68. Chen, You-Ren, "Dynamic Traffic Light Optimization and Control System using Model-Predictive Control Method," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2015.
69. Hsieh, Pei-Chi, "Model Predictive Optimization for Distribution Management in Smart Grid," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2015.
70. Wu, Wen-Hao, "Adaptive Timing Optimization for Cyber Physical Signal Control System," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2015.
71. Lee, Hsuan-Ru, "Software-Defined Monitoring for High Speed Network Flow Analysis in Network-on-Chip," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2015.
72. Tseng, Kwan-Wei, "Virtualization Architecture for Application-Oriented Reconfigurable Network-on-Chip System," National Chung Cheng University, Department of Computer Science and Information Engineering, June 2015.

18 Research Grants

18.1 Research Project Grants

1. *Formal Verification Methodology and Tool Design for System-on-a-Chip*, August 2001 to July 2002, Project Grant NSC 90-2215-E-194-009, NT\$438, 400.
2. *Design of a Synthesis Tool for Real-Time Embedded Software Development (1/3)*, August 2002 to July 2003, Project Grant NSC 91-2213-E-194-008, NT\$776, 600.
3. *Design of a Formal Verification Tool for SoC*, August 2002 to July 2003, Project Grant NSC 91-2215-E-194-008, NT\$597, 200.
4. *Design of a Synthesis Tool for Real-Time Embedded Software Development (2/3)*, August 2003 to July 2004, Project Grant NSC 92-2213-E-194-003, NT\$744, 200.
5. *Hardware-Software Codesign and Coverification of a Tunable SoC platform (I)*, August 2003 to July 2004, Project Grant NSC 92-2218-E-194-009, NT\$559, 400.
6. *Design of a Synthesis Tool for Real-Time Embedded Software Development (3/3)*, August 2004 to July 2005, Project Grant NSC 93-2213-E-194-002, NT\$725, 800.
7. *Design and Implementation of a Real-Time Operating System for Scalable Low-Power Custom Embedded Systems*, August 2005 to July 2006, Project Grant NSC 94-2215-E-194-005, NT\$822, 000.
8. *Design and Implementation of a Synthesis and Verification Tool for Real-Time Embedded Software*, February 2006 to January 2007, Project Grant NSC 95-3113-P-194-002, NT\$863, 000.
9. *Design and Implementation of an Operating System for Reconfigurable Systems (I)*, August 2006 to July 2007, Project Grant NSC 95-2221-E-194-095, NT\$789, 000.
10. *Design and Implementation of an Operating System for Reconfigurable Systems (II)*, August 2007 to July 2009, Project Grant NSC 96-2221-E-194-065-MY2, NT\$2, 356, 000.
11. *Synthesis and Code Generation of Multi-Core Embedded Software*, August 2008 to July 2009, Project Grant NSC 97-2218-E-194-002, NT\$906, 000.
12. *REALIFE-CR: A REasoning And Learning with Intelligent FPGA Embedded CR Platform*, Sub-Project 4: Design and Implementation of a REasoning And Learning (REAL) Framework for Cognitive Radio, November 2007 to October 2010, Project Grant NSC 96-2220-E-002-032.
13. *Synthesis and Code Generation of Multi-Core Embedded Software (VMC_SYN)*, August 2009 to July 2011, Project Grant NSC 98-2220-E-194-008, NT\$1, 858, 000.
14. *Design and Implementation of Architecture and Programming Models for Dynamically Reconfigurable Hardware-Software Systems*, August 2009 to July 2012, Project Grant NSC 98-2221-E-194-049-MY3, NT\$2, 853, 000.
15. *Safety and Security Analysis of Safety-Critical Systems*, January 2010 to December 2010, INER, NT\$630, 000.

16. *Design and Implementation of a Reconfigurable Multicore Architecture*, August 2012 to July 2015, Project Grant NSC 101-2221-E-194-060-MY3, NT\$3,843,000.
17. *Design and Implementation of an Application Framework for Model-Driven Development of Heterogeneous Multi-Core Software*, August 2012 to July 2013, Project Grant NSC 101-2221-E-194-023, NT\$483,000.
18. *Smart City Virtualization and Modeling*, August 2013 to July 2014, Project Grant NSC 102-2221-E-194-038, NT\$800,000.
19. *Micro Grid System Design Modeling and Simulation*, September 2013 to May 2014, INER, NT\$700,000.
20. *Model-Predictive Control and Optimization Design for Smart Grids*, August 2014 to July 2015, MOST 103-2221-E-194-035, NT\$706,000.
21. *Integrating Creative Teaching into Capstone Course*, December 2014 to November 2017, MOST 103-2511-S-194-004-MY3, NT\$2,632,000.
22. *Design and Implementation of a Smart Development Platform for Cyber-Physical Systems*, August 2015 to July 2016, MOST 104-2221-E-194-064, NT\$903,000.

18.2 Construction Project Grants

- *RFID-based Campus Security for Special Education School*, Ministry of Education, December 2008 to December 2009, NT\$4,010,000.
- *RFID-based Campus Security for Elementary and Special Education Schools*, Ministry of Education, December 2009 to December 2010, NT\$5,328,000.

18.3 Educational Reform Project Grants

- *System-on-Chip Design Flow and Tools*, SoC System-Level Design (SLD) Consortium, Ministry of Education, Taiwan, Course Planning and Development, since 2004.
- *Software Quality Management*, Software Engineering Consortium, Ministry of Education, Taiwan, Course Planning and Development, since 2005.
- *Software Engineering*, Software Engineering Consortium, Ministry of Education, Taiwan, Course Reformation, 2005.
- *Embedded Software Laboratories for Undergraduates*, Embedded Software Consortium, Ministry of Education, Taiwan, Course Planning and Development, 2005 ~ 2007.
- *Embedded System Programming*, Embedded Software Consortium, Ministry of Education, Taiwan, Course Reformation, 2006/12 ~ 2008/01.
- *System-on-Chip SoC Consortium*, Ministry of Education, Taiwan, Course Reformation, 2007–2009.
- *Reconfigurable System Prototype Design and Applications*, Prototyping and Layout Consortium, Ministry of Education, Taiwan, Course Planning and Development, 2008/3 ~ 2009/02.

- *Reconfigurable System Prototype Design and Applications*, ATP Consortium, Ministry of Education, Distance Learning Course Materials, Taiwan, 2009/3 ~ 2010/02.
- *Internet of Things*, Network Communications Consortium, Ministry of Education, Taiwan, 2012/02~2014/01.
- *Software Personnel Training in Cloud Computing and Service*, Ministry of Education, Taiwan, 2012/02~2014/01.
- *Intelligent Electronics Training and Education in Medical Imaging Systems*, Ministry of Education, Taiwan, 2011/09~2014/01.

18.4 Workshop Organization Grant

- *International Workshop on Distributed System Validation and Verification*, April 2000, Taipei, Taiwan, NSC Grant NT\$400,000.

18.5 Travel Grants

1. *24th International Conference on Technology of Object-Oriented Languages and Systems (TOOLS'97)*, September 1997, Beijing, China, Academia Sinica Grant NT\$35,000.
2. *International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA'98)*, July 1998, Las Vegas, USA, Academia Sinica Grant.
3. *International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA'99)*, June 1999, Las Vegas, USA, Academia Sinica Grant.
4. *7th IEEE/ACM International Workshop on Hardware-Software Codesign (CODES'99)*, May 1999, Rome, Italy, Academia Sinica Grant.
5. *3rd IEEE International Symposium on High-Assurance Systems Engineering (HASE'98)*, November 1998, Washington D.C., USA, NSC Grant NT\$60,000.
6. *5th International Conference on Principles and Practice of Constraint Programming (CP'99)*, October 1999, Alexandria, Virginia, USA, NSC Grant NT\$69,000.
7. *7th IEEE International Conference on Real-Time Computing Systems and Applications (RTCSA'00)*, December 2000, Cheju Island, Korea, Academia Sinica Grant NT\$11,500.
8. *9th ACM/IEEE International Conference on Hardware-Software Codesign (CODES'01)*, April 2001, Copenhagen, Denmark, NCCU-CSIE Grant NT\$15,000.
9. *21st IFIP International Conference on Formal Techniques for Networked and Distributed Systems (FORTE'01)*, August 2001, Cheju Island, Korea, NSC Grant NT\$27,000.
10. *8th Asia-Pacific Software Engineering Conference (APSEC'01)*, December 2001, Macau SAR, China, CCU Grant NT\$30,000.
11. *8th International Conference on Real-Time Computing Systems and Applications (RTCSA'02)*, March 2002, Tokyo, Japan, MOE Grant NT\$18,000.

12. *5th IEEE International Symposium on Object-Oriented Real-Time Distributed Computing (ISORC'02)*, April 2002, Washington D.C., USA, NSC Grant NT\$39,000.

18.6 Speaker Grants

1. *7th IEEE/ACM International Workshop on Hardware-Software Codesign (CODES'99)*, May 1999, Rome, Italy, IEEE Grant US\$ 660.
2. *9th ACM/IEEE International Conference on Hardware-Software Codesign (CODES'01)*, April 2001, Copenhagen, Denmark, IEEE/ACM Grant US\$ 820.

19 Paper Refereeing

Pao-Ann Hsiung has been taking an active part in reviewing papers for international conferences and journals for quite a few years.

19.1 International Conferences

1. *Asian Conference on Computer Science (ASIAN)*,
2. *International Symposium on Hardware-Software Codesign and System Synthesis (CODES-ISSS)*,
3. *Design Automation Conference (DAC)*,
4. *European Conference on Real-Time Systems (ECRTS)*,
5. *International Conference on Distributed Computing Systems (ICDCS)*,
6. *International Conference on Real-Time Computing Systems and Applications (RTCSA)*,
7. *International Conference on Real-Time Applications and Systems (RTAS)*,
8. *Real-Time Systems Symposium (RTSS)*,
9. *International Workshop on Parallel and Distributed Real-Time Systems (WP-DRTS)*,
10. *International Conference on Parallel and Distributed Systems (ICPADS)*,
11. *International Symposium on Automated Techniques in Verification and Analysis (ATVA)*,
12. *Asia-Pacific Design Automation Conference (ASPDAC)*,
13. *Embedded and Ubiquitous Computing (EUC)*,
14. *Asian Symposium on Programming Languages and Systems (APLAS)*,
15. *VLSI Design / CAD Symposium (VLSI/CAD)*,
16. *..., and all those conferences in which I am a program committee member!*

19.2 International Journals

1. *ACM Transactions on Reconfigurable Technology and Systems* (TRETs),
2. *ACM Transactions on Design Automation of Electronic Systems* (TODAES),
3. *ACM Transactions on Embedded Computing Systems* (TECS),
4. *IEEE Transactions on Computers* (TC),
5. *IEEE Transactions on Computer-Aided Design* (TCAD),
6. *IEEE Transactions on Parallel and Distributed Systems* (TPDS),
7. *IEEE Transactions on Robotics and Automation* (TRA),
8. *IEEE Transactions on VLSI Systems* (TVLSI),
9. *IEEE Transactions on Systems, Man, and Cybernetics* (TSMC),
10. *INFORMS Journal on Computing* (JoC),
11. *International Journal of System Architecture* (JSA),
12. *Journal of Computer Science and Technology* (JCST),
13. *Journal of Information Science and Engineering* (JISE), Taiwan,
14. *Journal of Signal Processing Systems* (JSPS),
15. *Journal of Supercomputing*, Kluwer Academic Publishers,
16. *Journal of Systems and Software* (JSS),
17. *Journal of Electronic Testing – Theory and Applications* (JETTA),
18. *IT Professional*,
19. *Formal Methods in System Design* (FMSD),
20. *International Journal of Foundations of Computer Science* (IJFCS),
21. *Design Automation for Embedded Systems* (DAES),
22. *Engineering Applications of Artificial Intelligence* (EAAI), Elsevier,
23. *The Computer Journal*, Oxford Journals, Oxford University Press, UK.