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Special Issue On

Hardware-Software Codesign for Systems-on-Chip

(<http://www.cs.ccu.edu.tw/~pahsiung/ijes-codesign/>)

(Deadline Extended: December 15, 2003)

With the rapidly permeating global trend of adopting SoC (System-on-Chip) design technologies, traditional hardware-software codesign techniques need adaptation and revamping to satisfy the growing needs of complex system designs. This special issue is devoted to presenting state-of-the-art SoC codesign and coverification methodologies, languages, techniques, tools, system architectures, and related technologies. Prospective papers should be unpublished and present solid research work offering innovative contributions either from a methodological or application point of view.

Topics of interest include (but are not limited to):

- Design & Verification Methodologies
- Design & Verification Languages
- Design & Verification Tools
- SoC Architectural Issues
- SoC Physical Impact on Codesign
- Nanotechnology and Codesign
- Mixed-Signal in Codesign
- Soft/Hard IP-reuse in Codesign
- Embedded Software Issues
- Embedded Hardware Issues
- Communication Issues
- Cosimulation Techniques
- (Semi)-Formal Verification
- Platform-Based Codesign Issues

Prospective authors should follow the Inderscience IJES manuscript format described at the Journal site <http://www.inderscience.com/catalogue/e/ijes/indexijes.html>. An electronic copy of the complete manuscript in PDF format is to be submitted by e-mail to **Pao-Ann Hsiung** at hpa@computer.org, according to the following schedule.

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