晶片系統設計流程與工具
SoC Design Flow & Tools

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Class: EA-101
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What will you learn from this course?

- What is a System-on-Chip (SoC)?
  - Motivation
  - History
  - State-of-Art

- What are the design issues?
  - Complexity: digital, analog, mixed, IP, memory, ...
  - Hardware-software codesign
  - Functional Verification: full-chip, hw, sw, ...

- How to design and verify an SoC?
  - Design & Verification Flow
  - Design & Verification Tools
Who should take this course?

• Interested in becoming a system (hardware-software) engineer
• Interested in designing SoCs
• EE background: learn system design, embedded software design, verification
• CS background: learn SoC architecture, embedded hardware design, verification
• Essential backgrounds: C/C++ programming, computer architecture, OS
Who should NOT take this course?

- Only wants course credits
- Only because SoC is popular
- Does not like research
- Does not like projects
- Does not like using tools or lab work
- Not creative (lack of new ideas)
- Yawns and goes to sleep when someone is talking about system design
Reference Books (Design)

Reference Books (Verification)


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Course Grading

• Mid-Term Exam 30%
• Final Exam 30%
• Digital Camera Project 20%
• Labs 20%
• Bonus: class Q/A, quiz, attendance, etc.
Digital Camera Project

• Design a digital camera SoC with hardware and software (JPEG)

• Schedule
  – Presentation Dec 23, 30, 2003
  – Demonstration Before Final Exam

• Grade: (total 20%)
  – Report 6%, Presentation 6%, Demo 8%
Labs

• Familiarity with Tools
  – Cadence SystemC/Verilog/VHDL simulators
  – Mentor Seamless Co-Verification Environment (CVE)
  – Altera Quartus II v3.0
  – Altera SoPC with Excalibur Stripe
  – Cadence Signal Processing Workstation (SPW)
  – ARM AMBA 2.0 TVM
Labs

• Choose 4 out of 6 labs (total 20%)
  – Assignment last ½ hour
  – Deadline after 2 weeks
  – Grading faster ➔ higher grades
  – Demonstration contact TA
  – TA = 吳展奇, Ext. 23125, Lab EA305
SoC Design Flow & Tools

ENJOY THE COURSE!!!