How do I use all this?

Outline

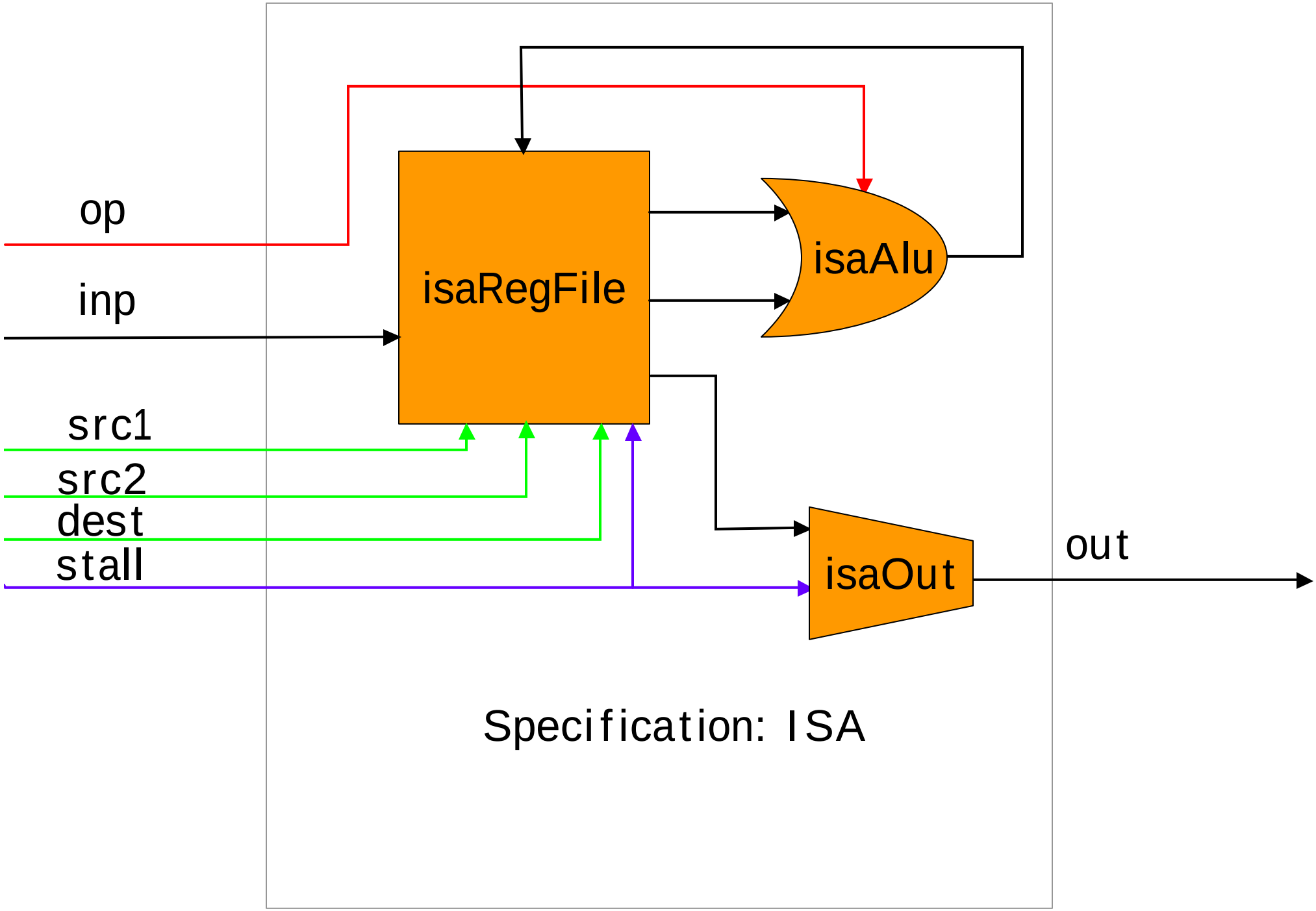
1 Informal Introduction

2 Formal Definitions

- Reactive Systems
- Witnessed Refinement Proofs
- Slicing Reactive Systems
- Decomposing Refinement Proofs

3 Formal Example: Three-Stage Pipeline

4 Informal Example: Dataflow Processor Array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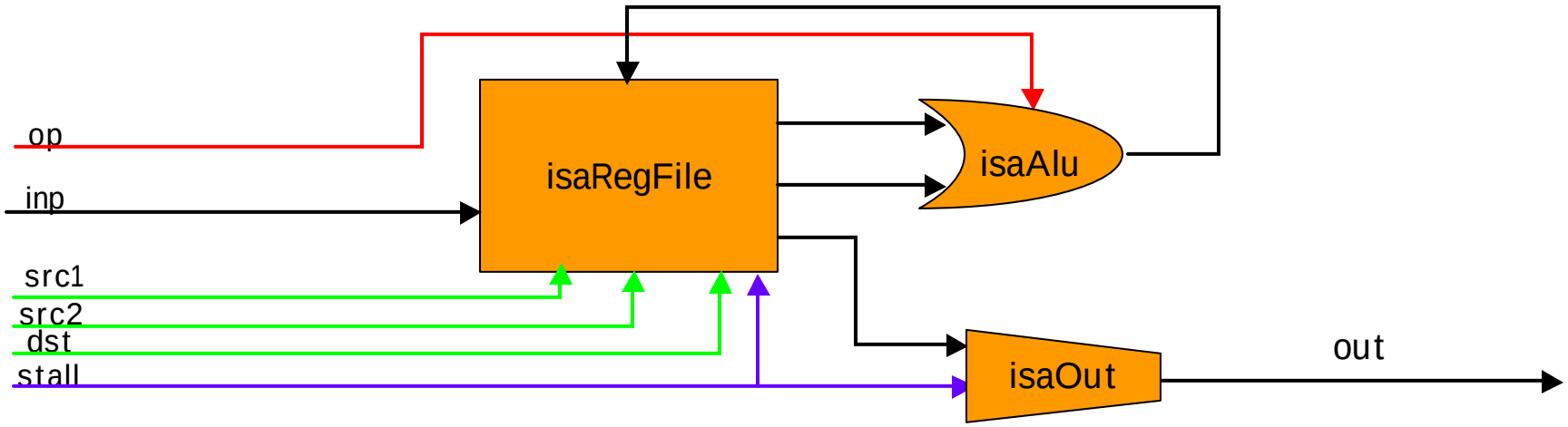
inp
src1
src2
dest
stall
isaRegFile
isaAlu
isaOut
out
Specification: ISA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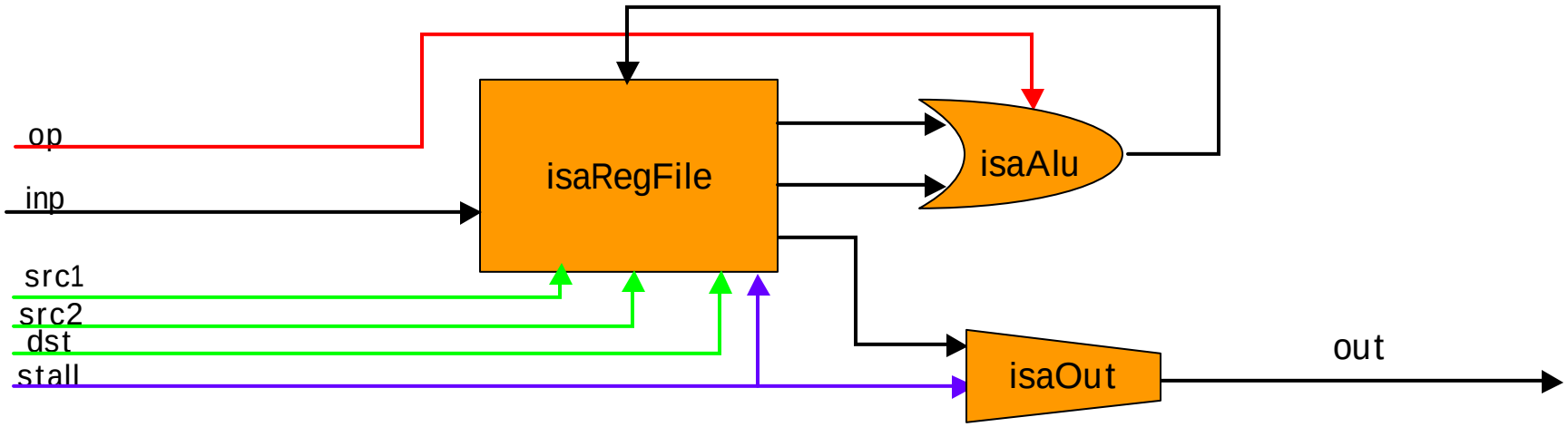
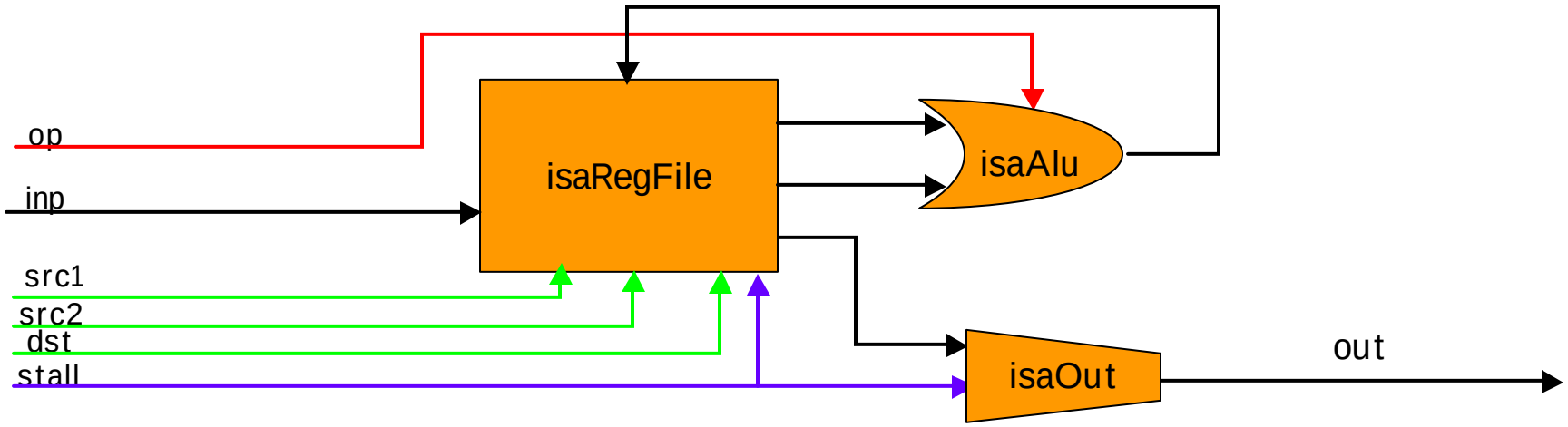
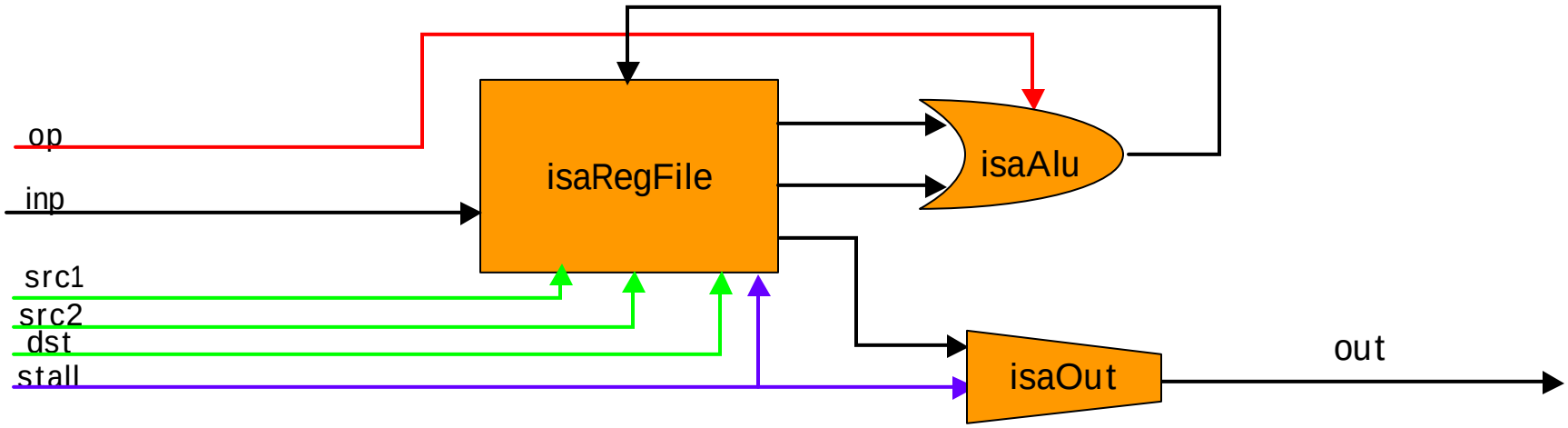
isaRegFile
isaAlu
isaOut
out




```
load    r1  1
xnor    r2  r1  r1
store   r2
```



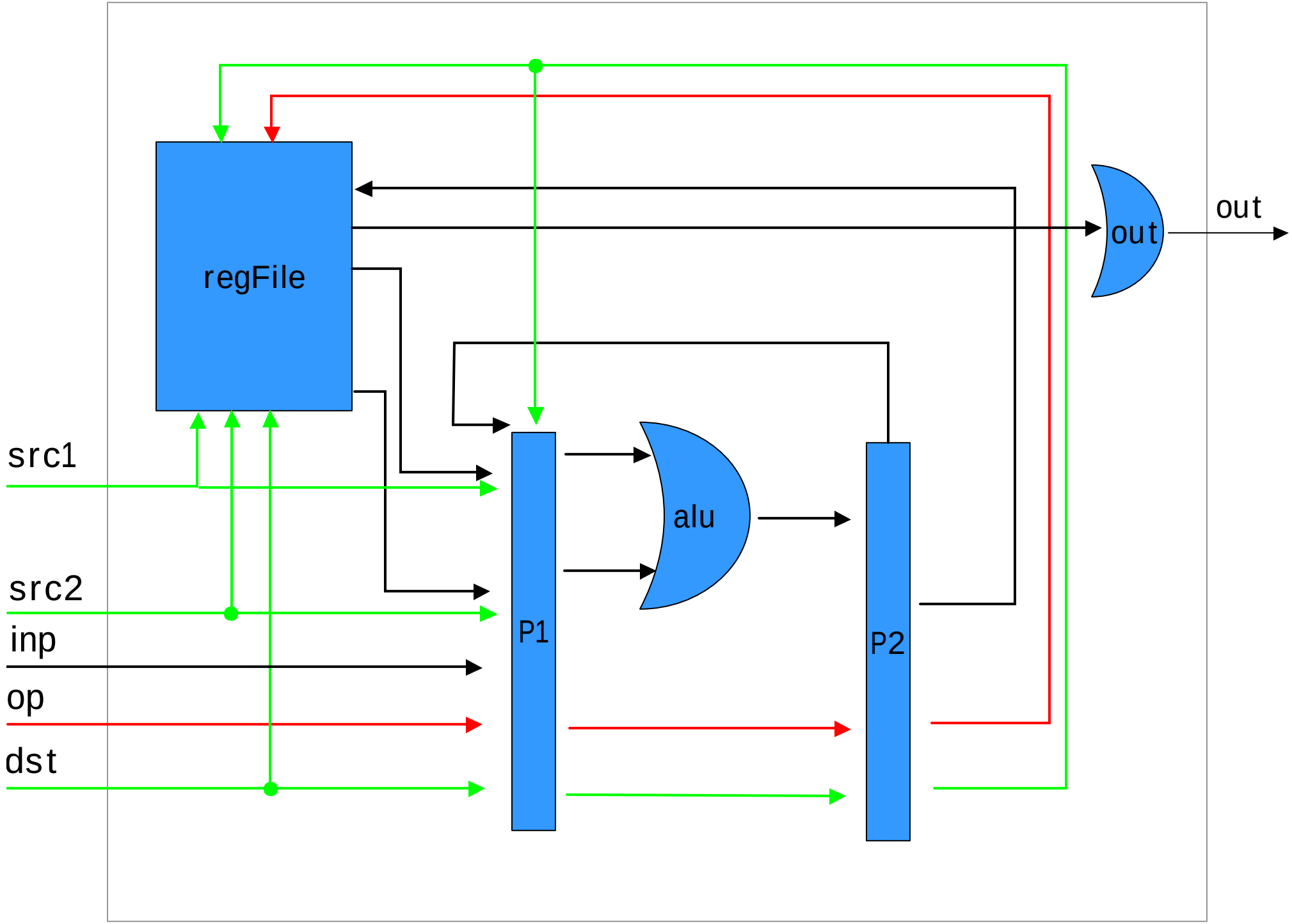
load	r1	1		r1	:=	1
xnor	r2	r1	r1	r2	:=	0
store	r2			out	:=	0



load	r1	1		r1 :=	1
xnor	r2	r1	r1	r2 :=	0
store	r2			out :=	0

Notes:

1. Store instruction results in an output
2. Memory hierarchy is not represented
3. Why do we need "stall" ?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out
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P2
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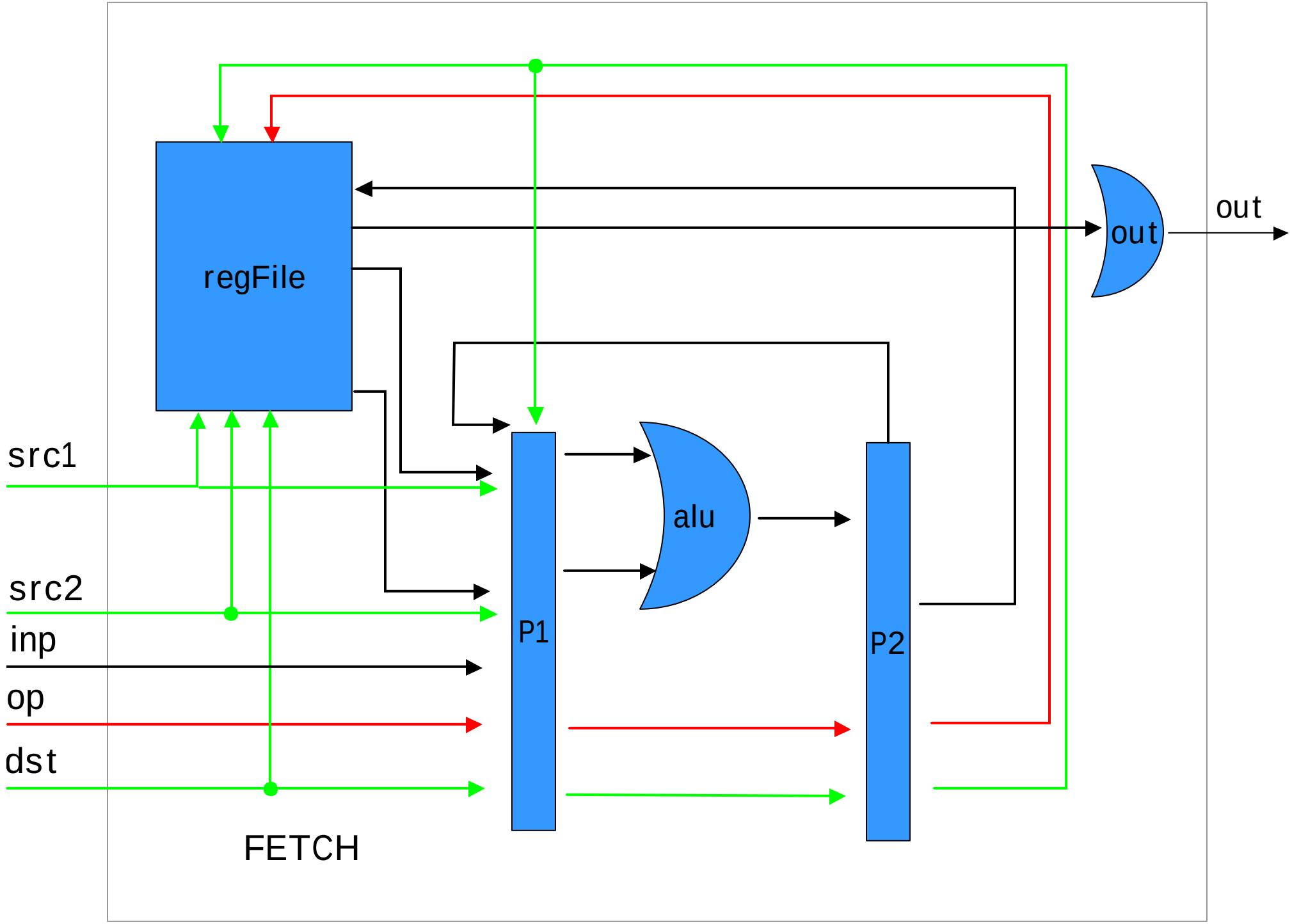
op
dst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out
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P1
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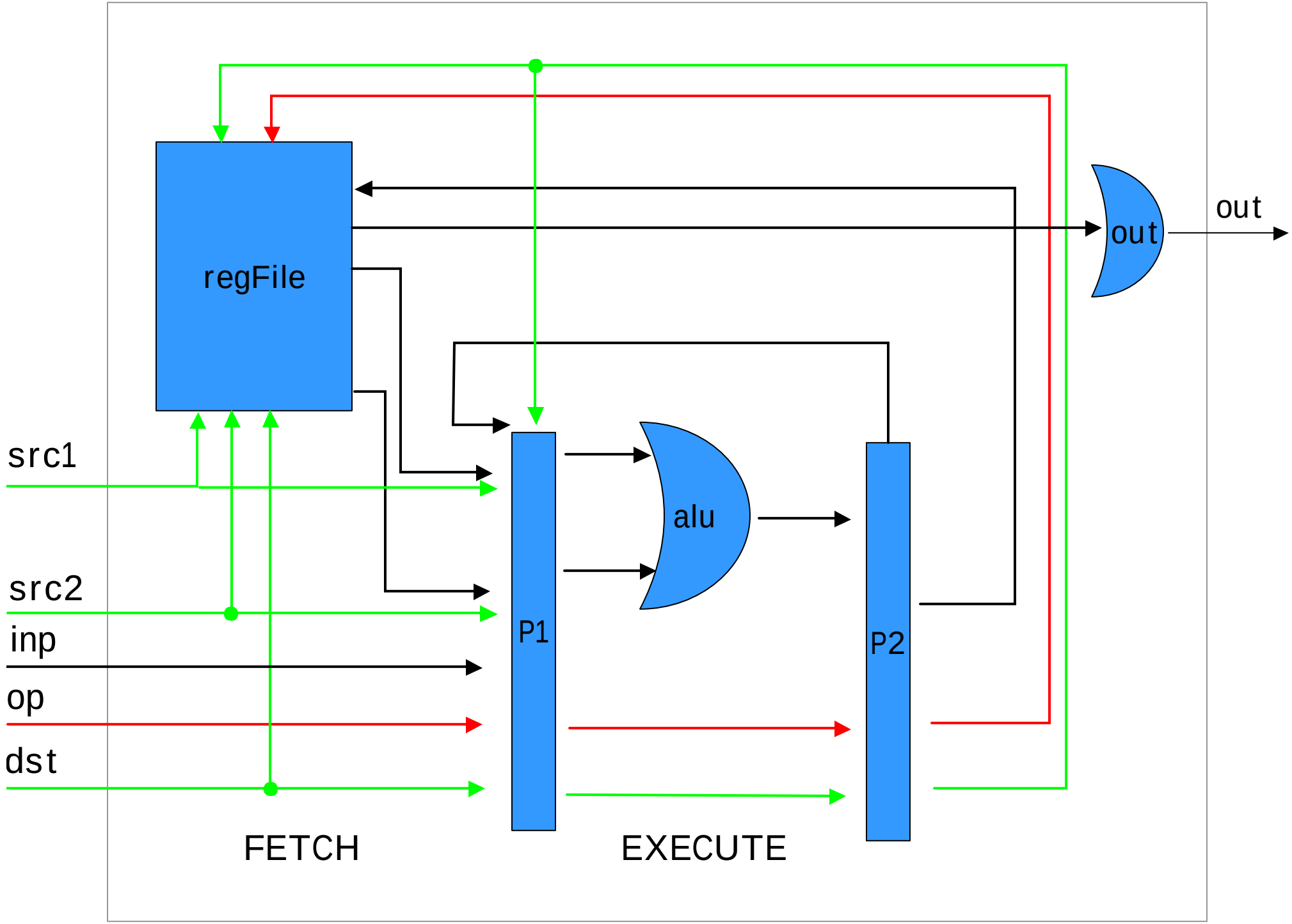
op
dst
FETCH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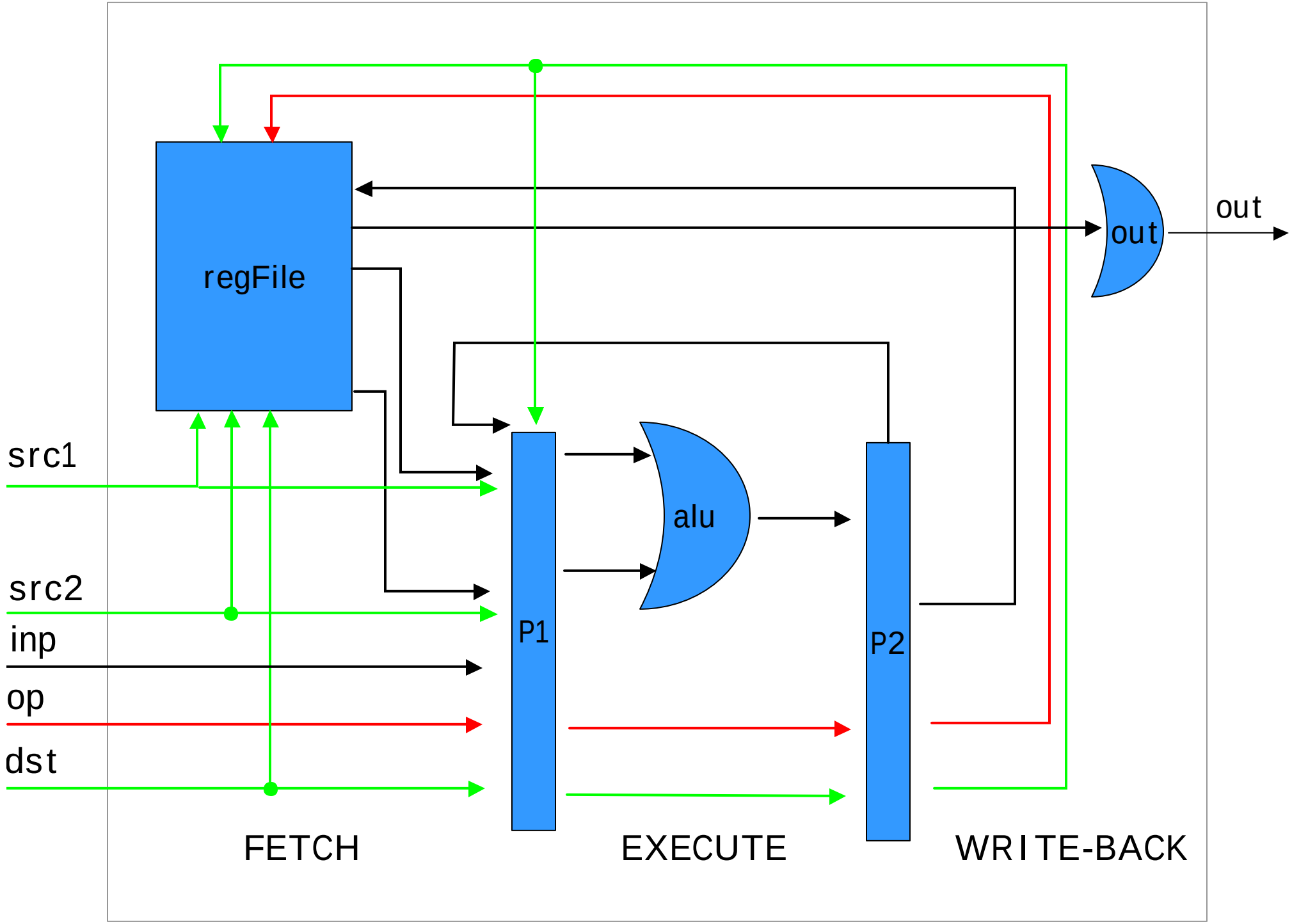
FETCH
EXECUTE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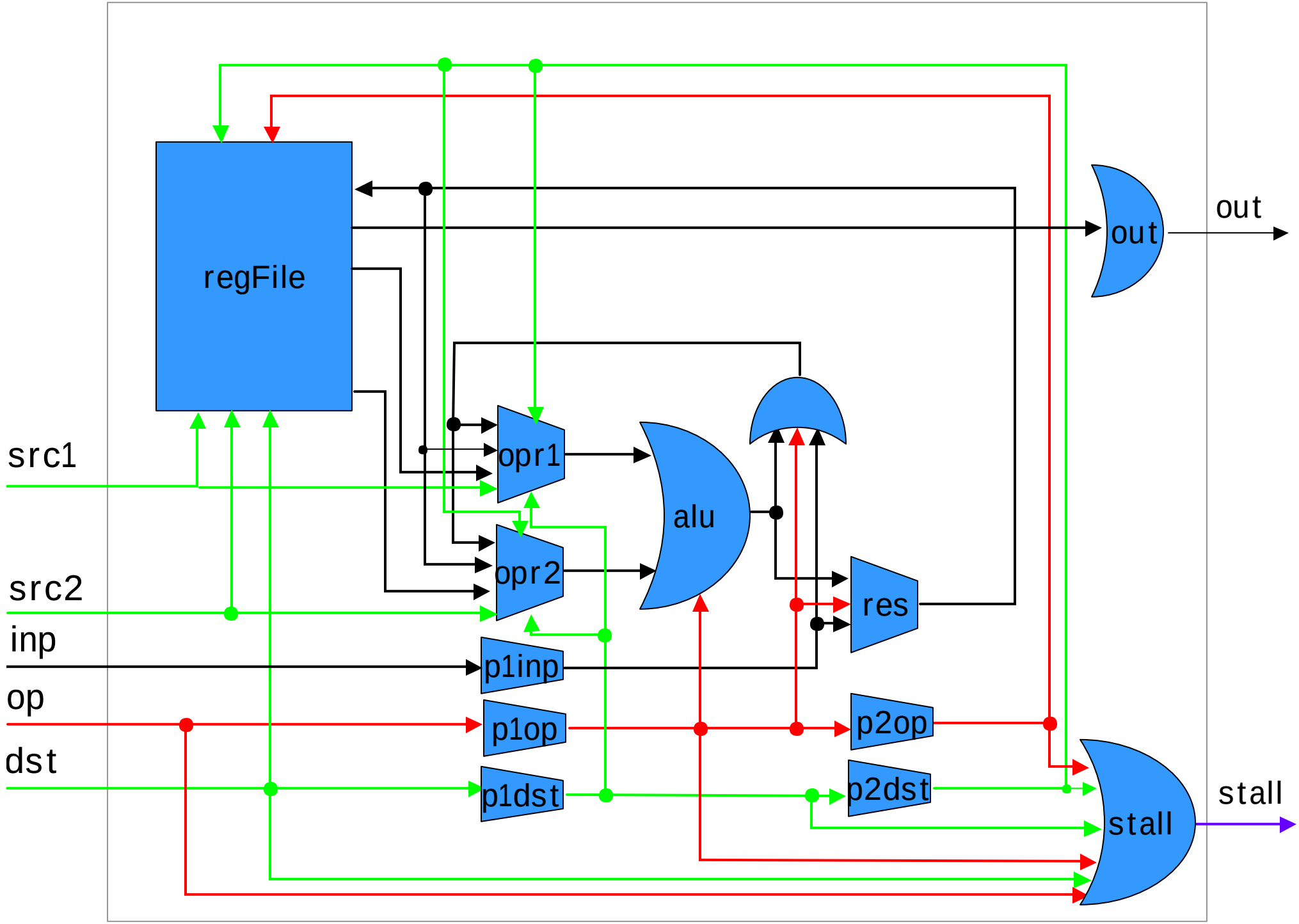
alu
P1
P2
FETCH
EXECUTE
WRITE-BACK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out
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opr1
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p2op
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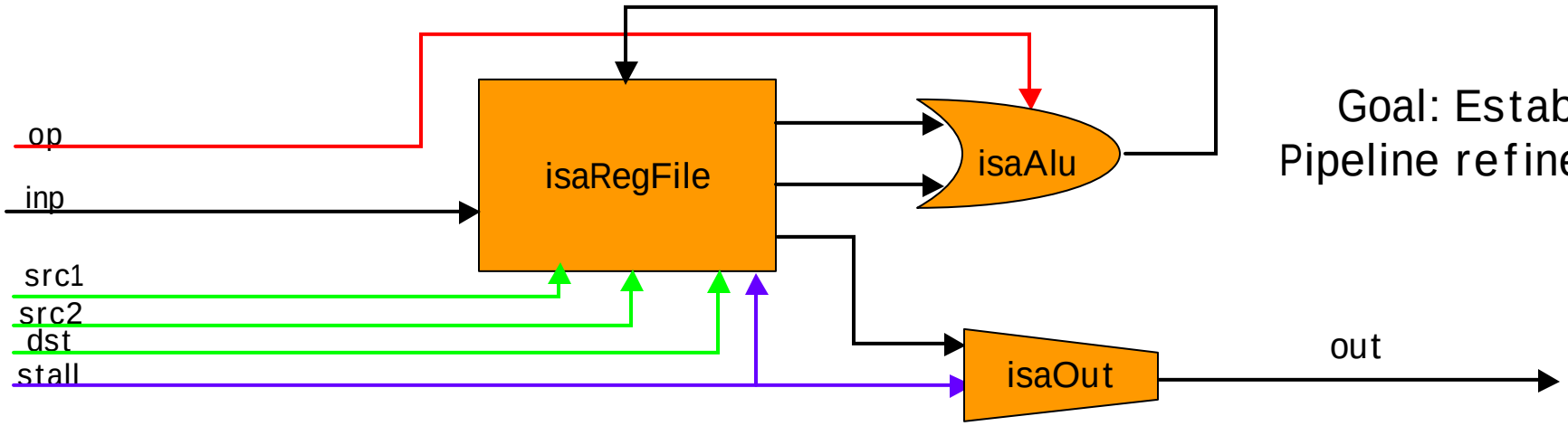
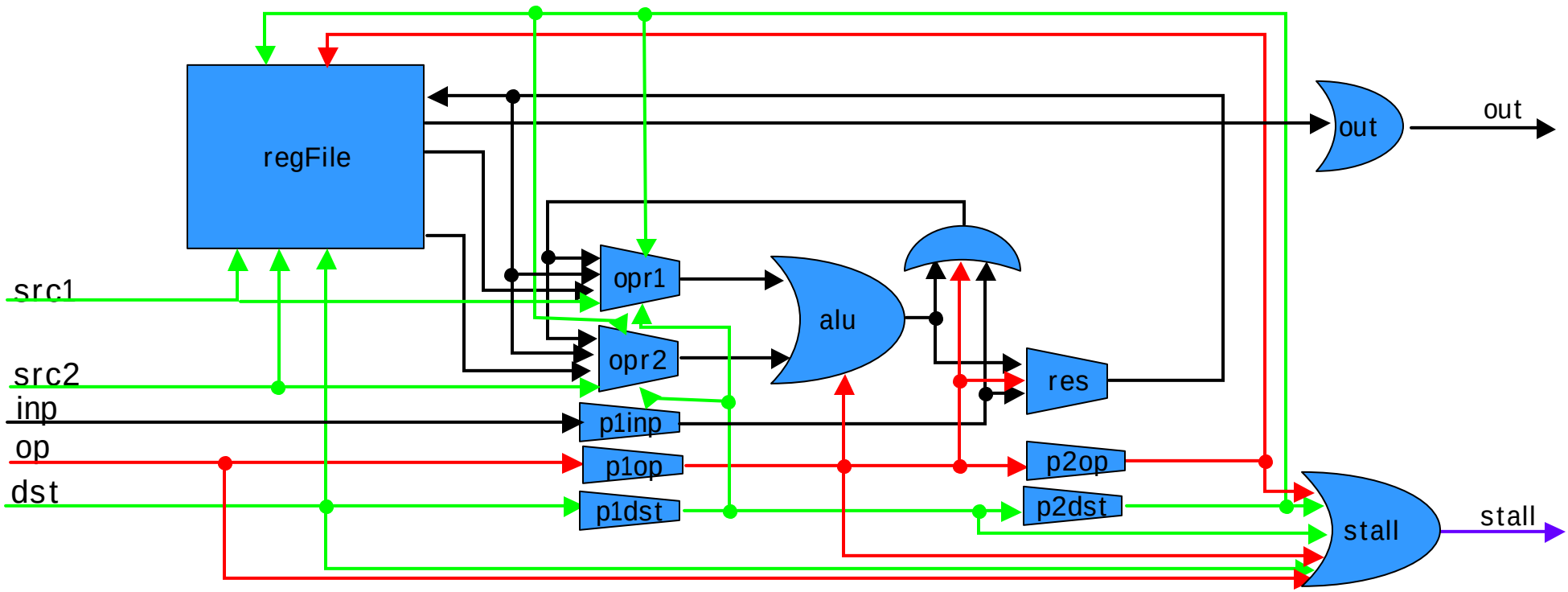
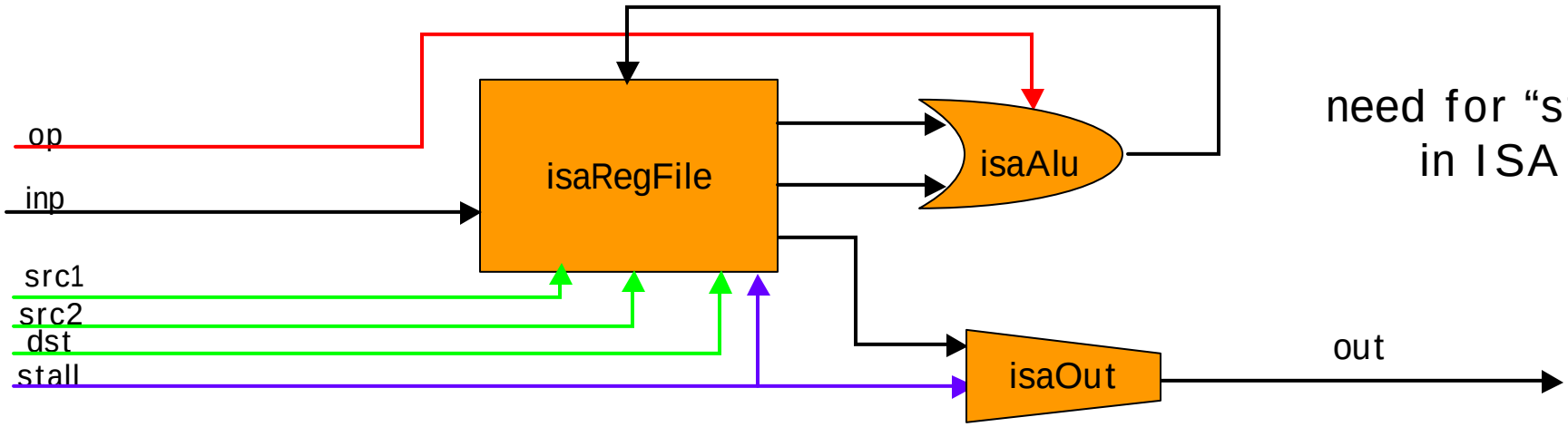
stall
stall

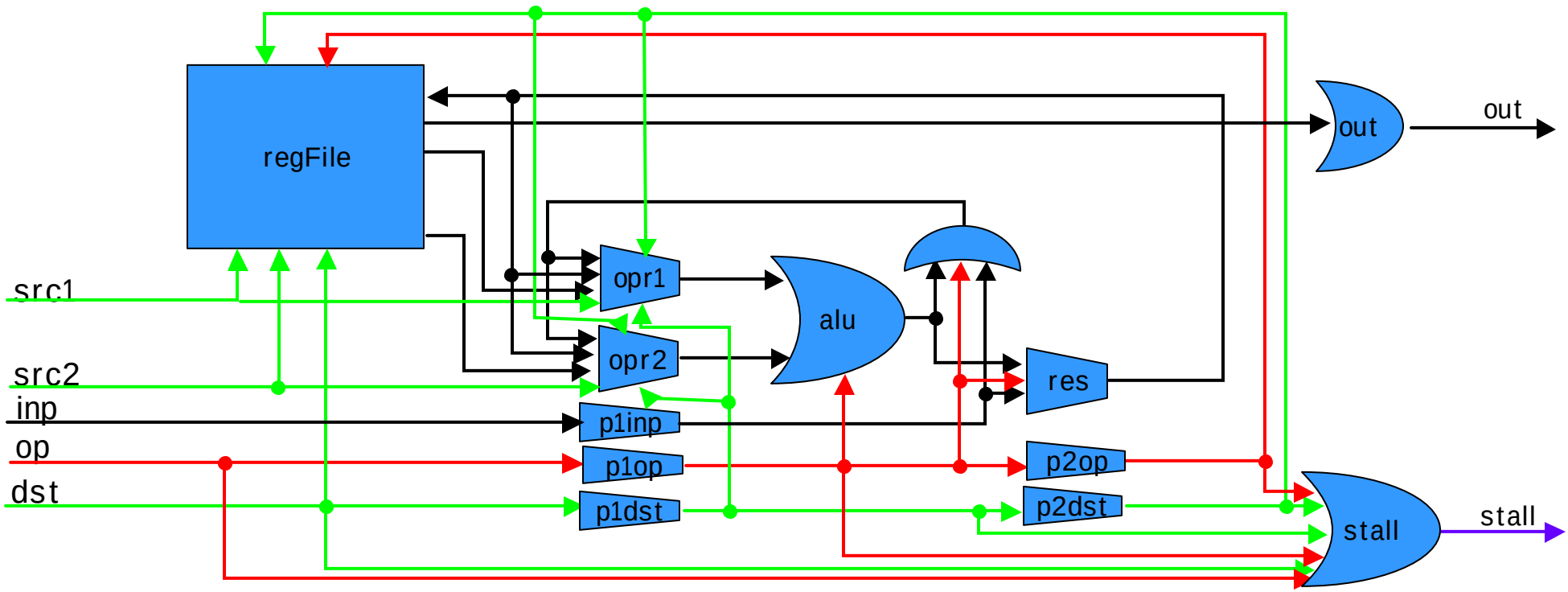


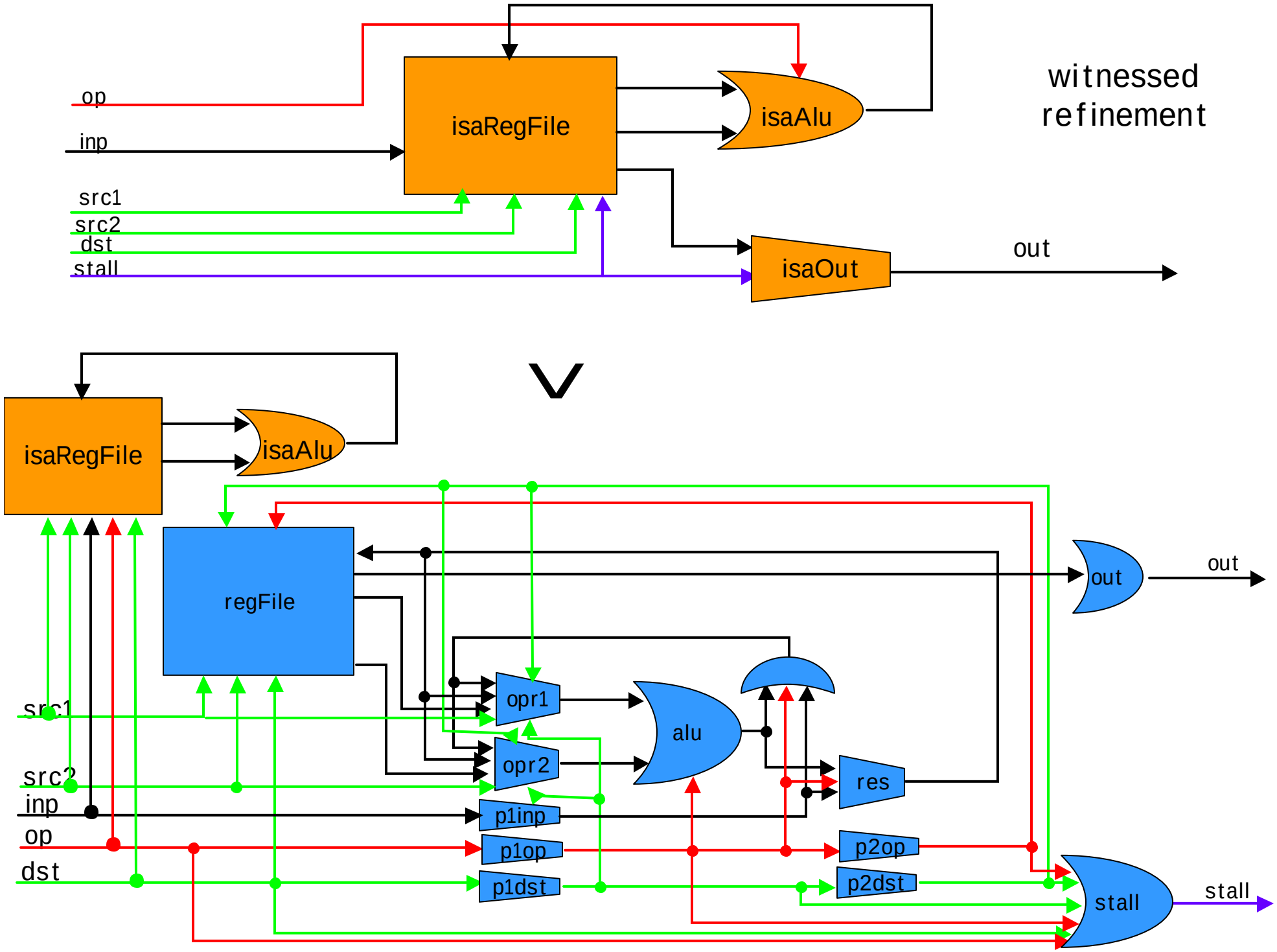
Goal: Establish
Pipeline refines ISA





need for “stall” in ISA




witnessed refinement
op
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isaOut
out
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isaRegFile
isaAlu
regFile
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out
opr1
opr2
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p1op
p1dst
p2op
p2dst
stall
stall
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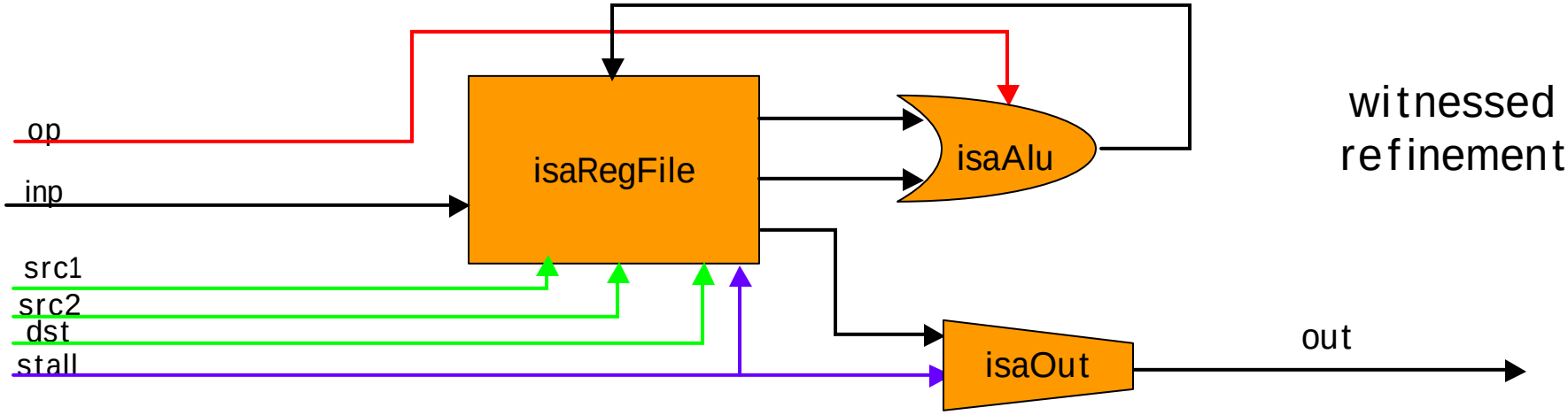
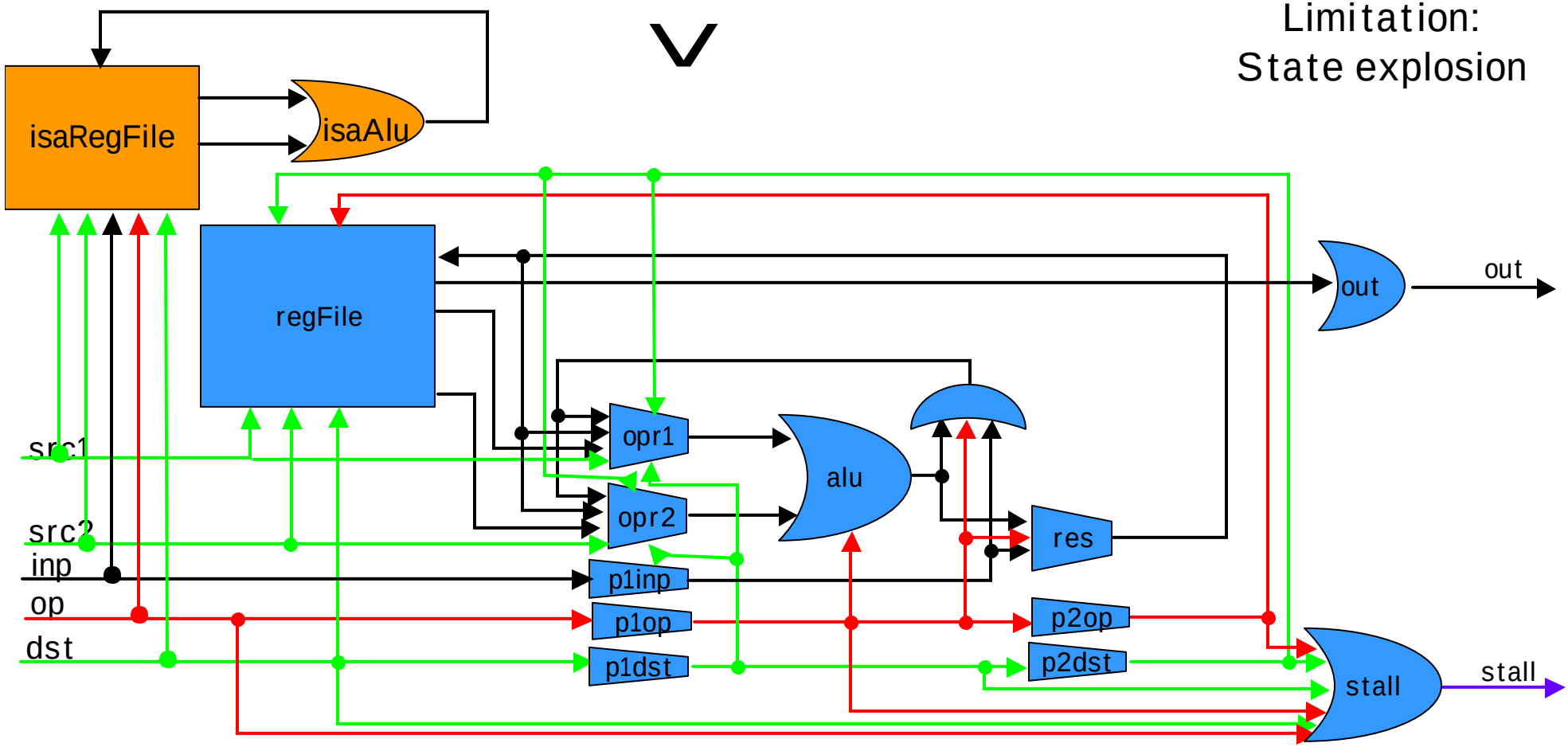
op
dst

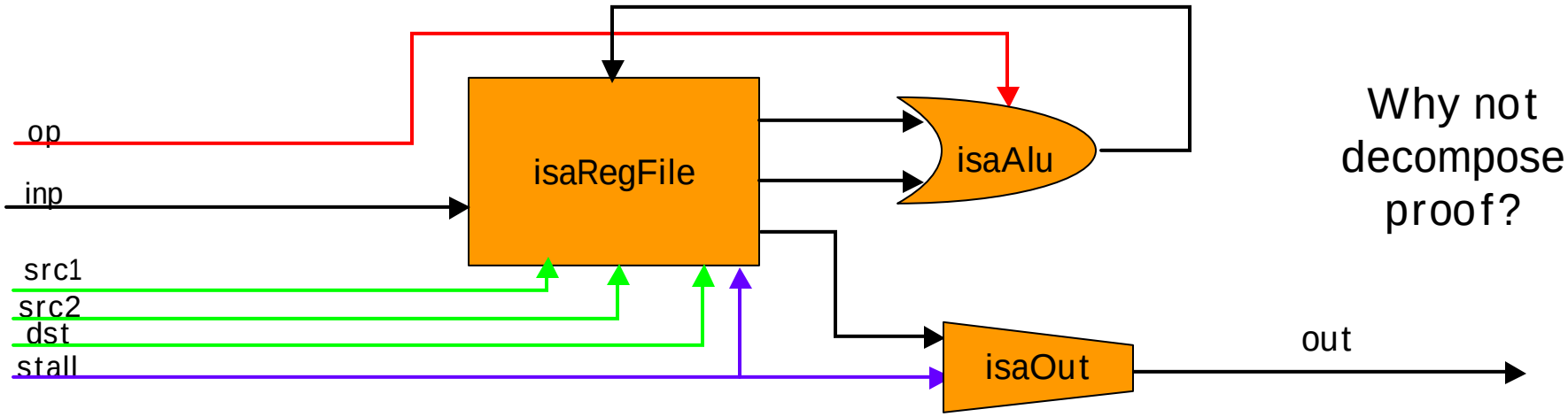


witnessed refinement

V

Limitation: State explosion

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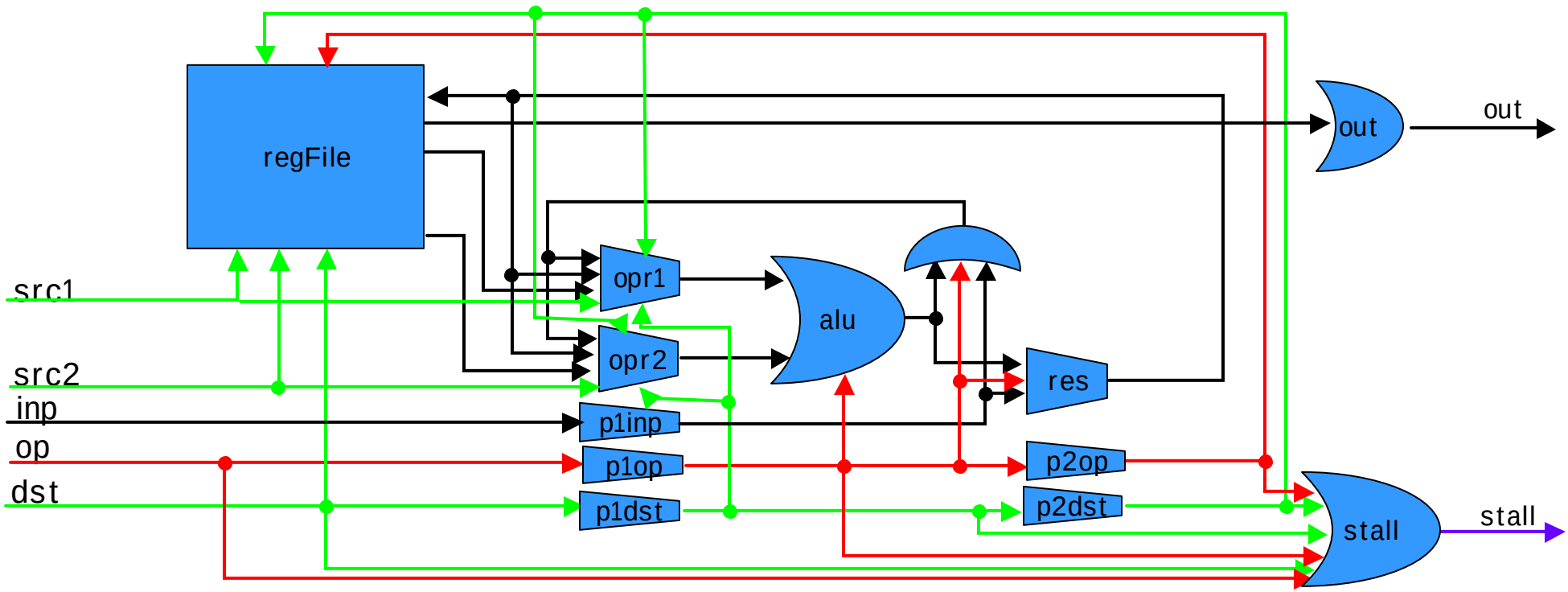
isaAlu
isaOut
out
Why not decompose proof?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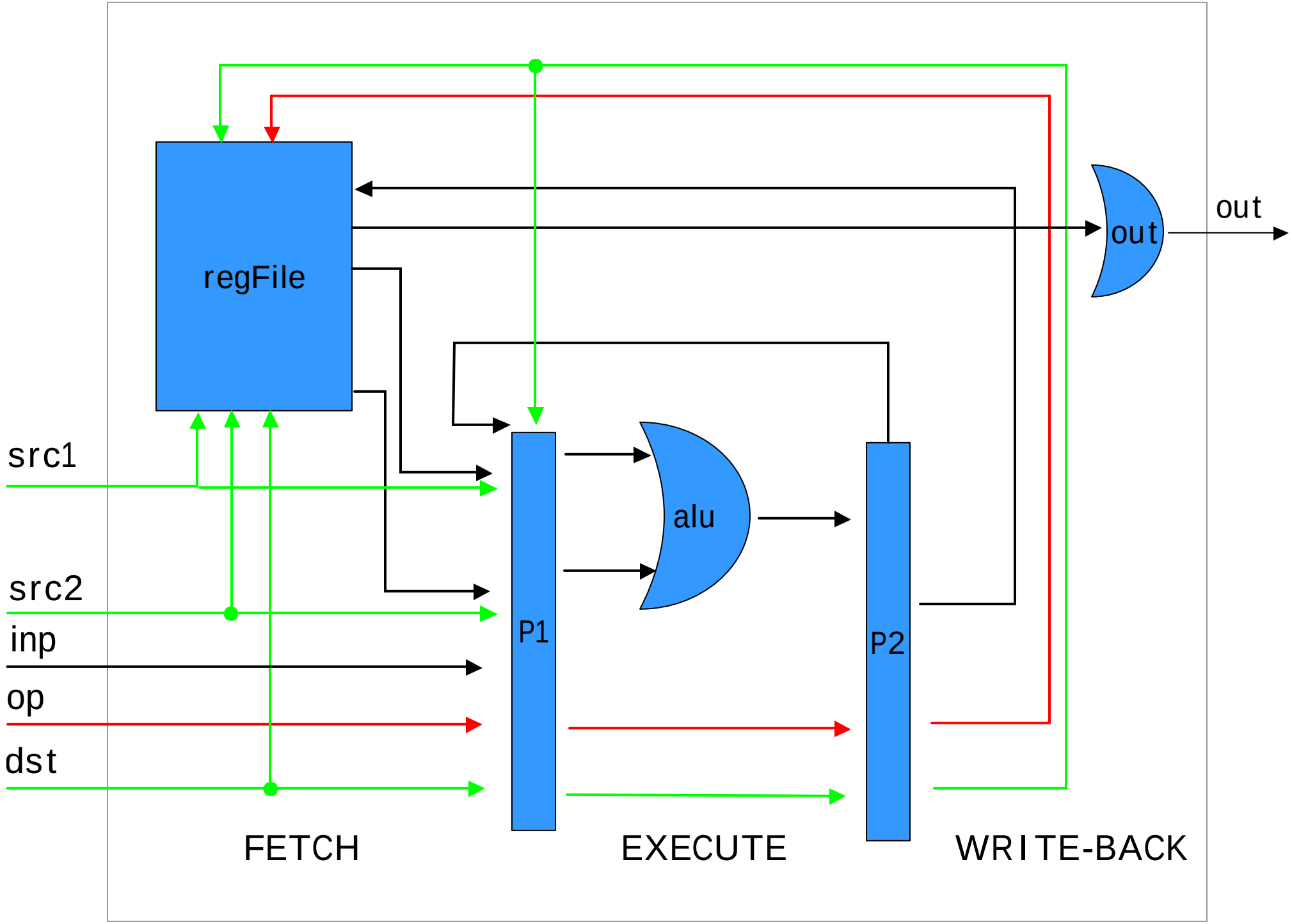
stall
stall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P2
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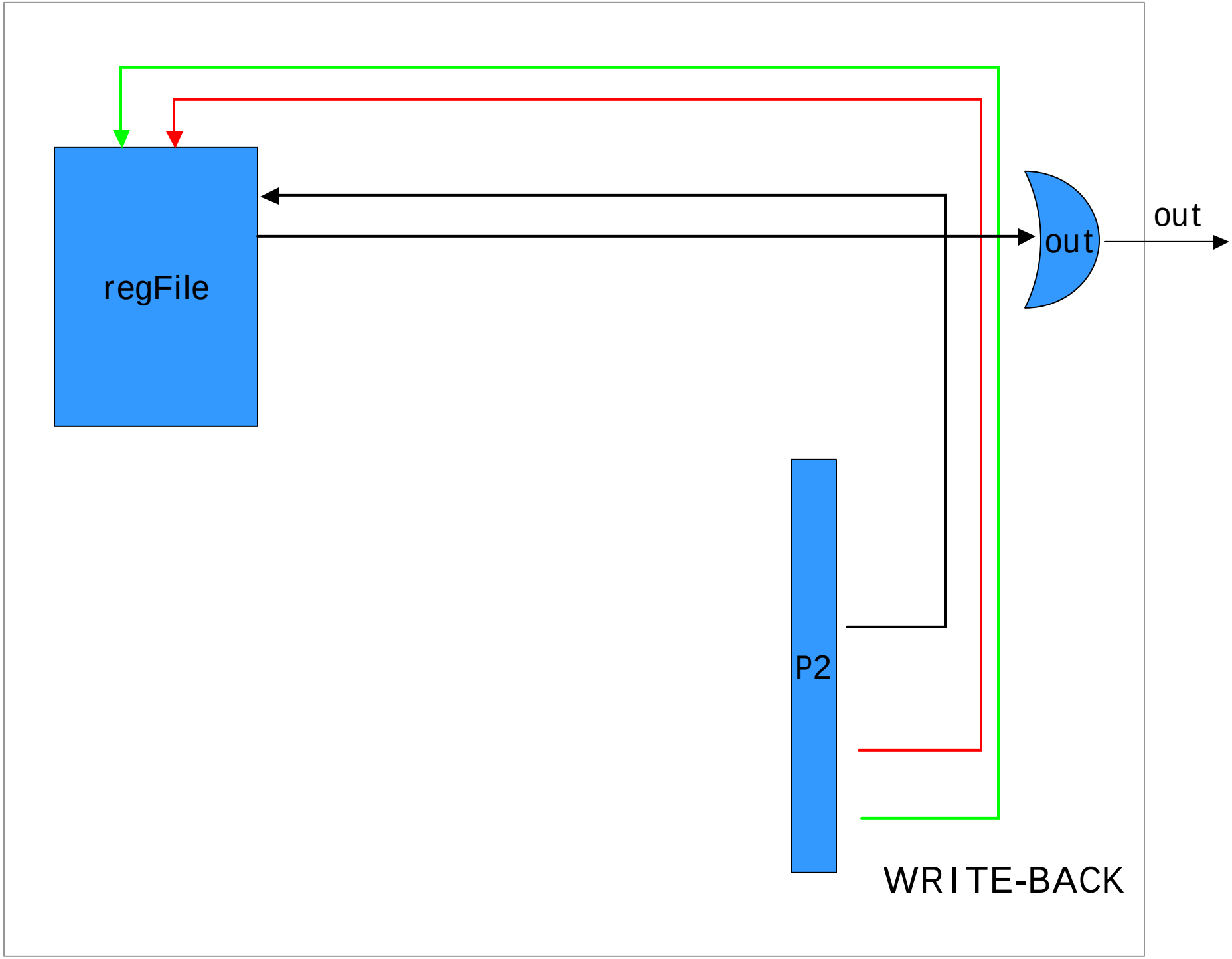
EXECUTE
WRITE-BACK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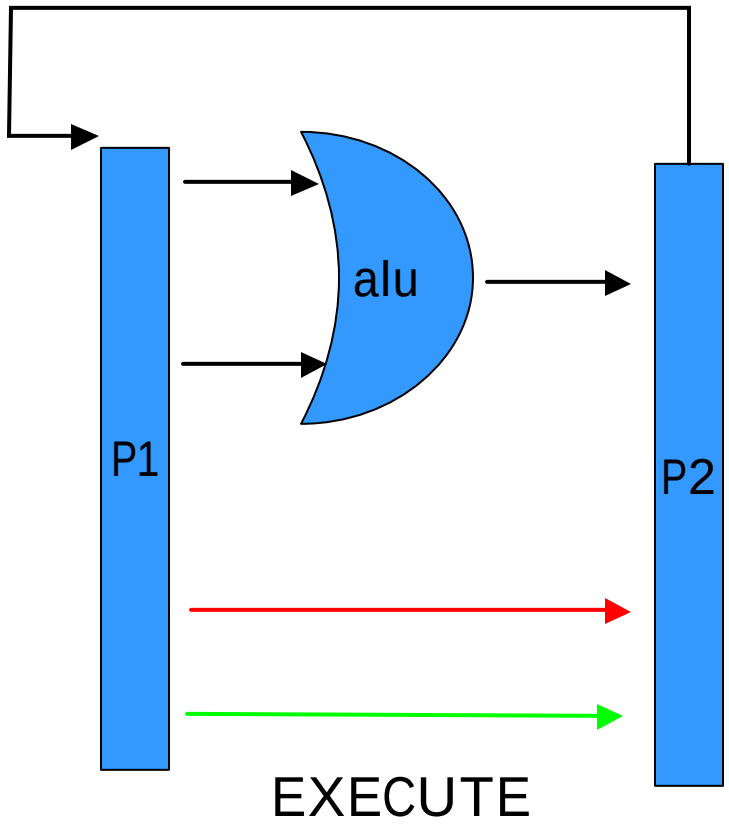
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P1
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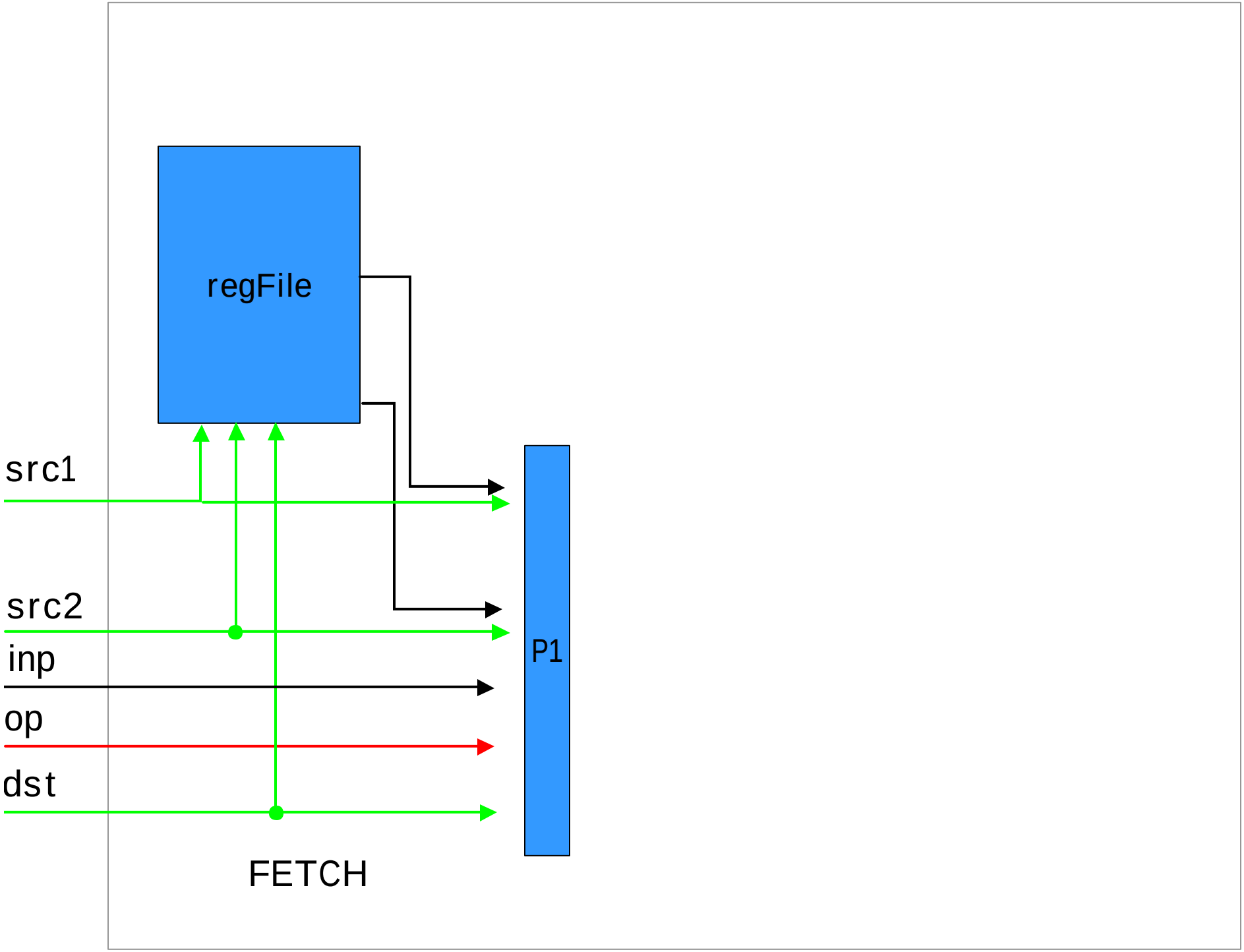
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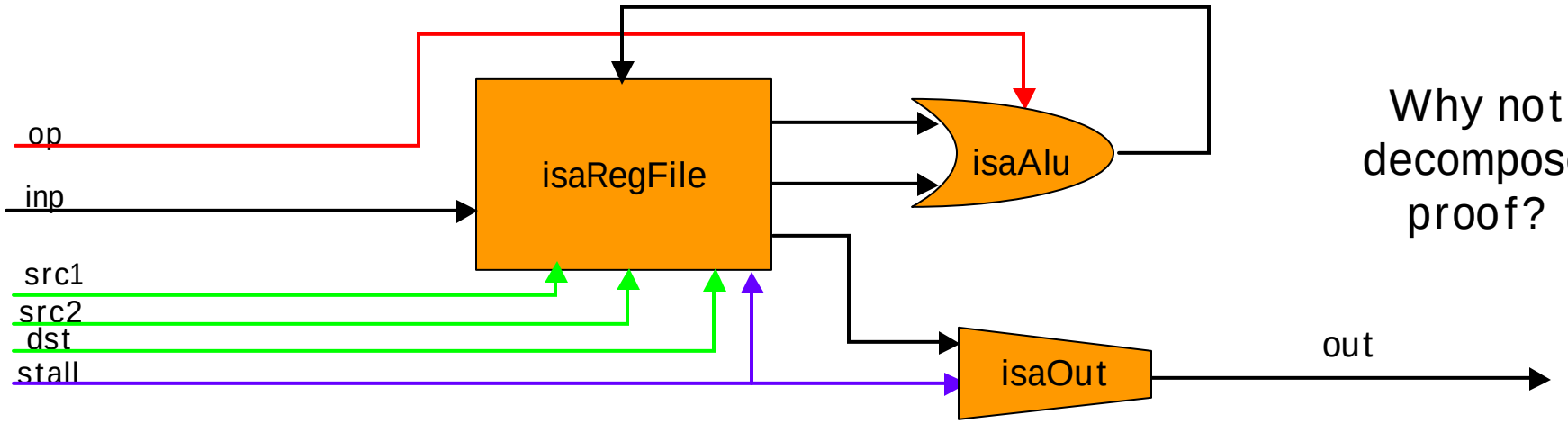
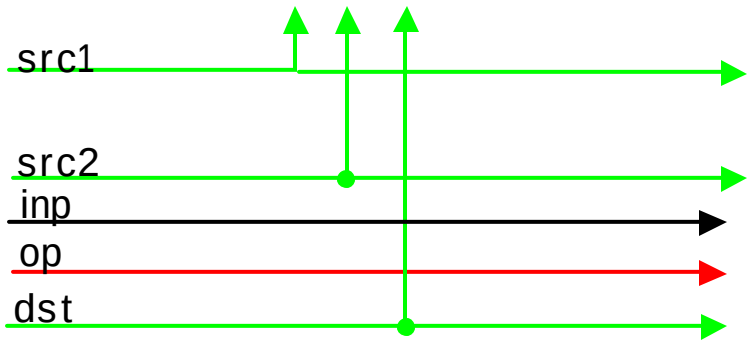
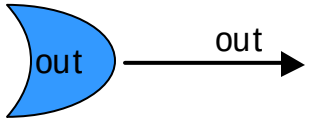
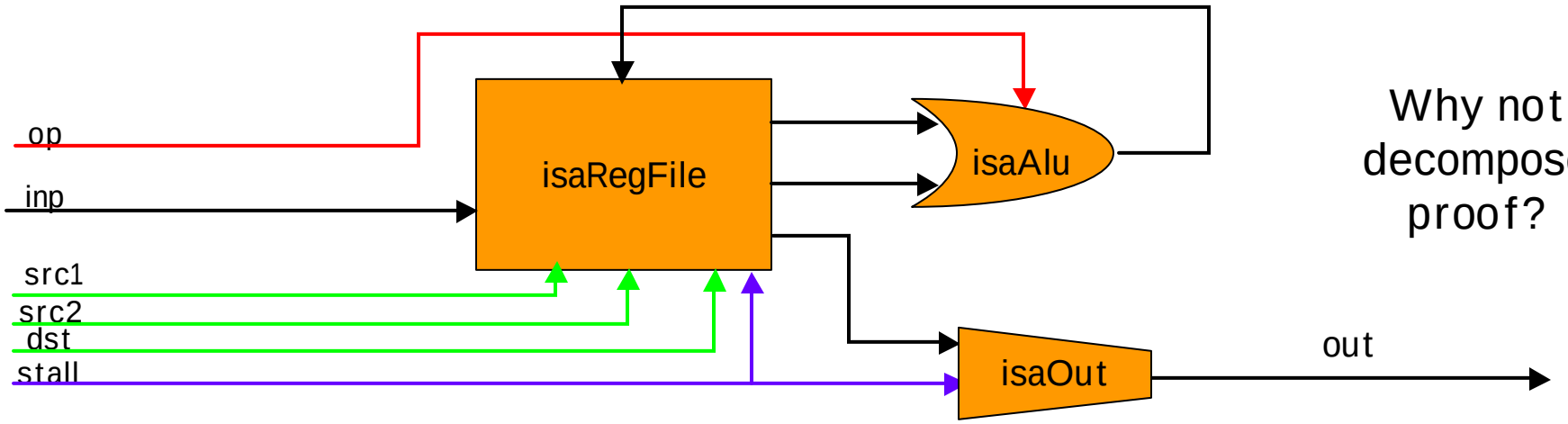
FETCH



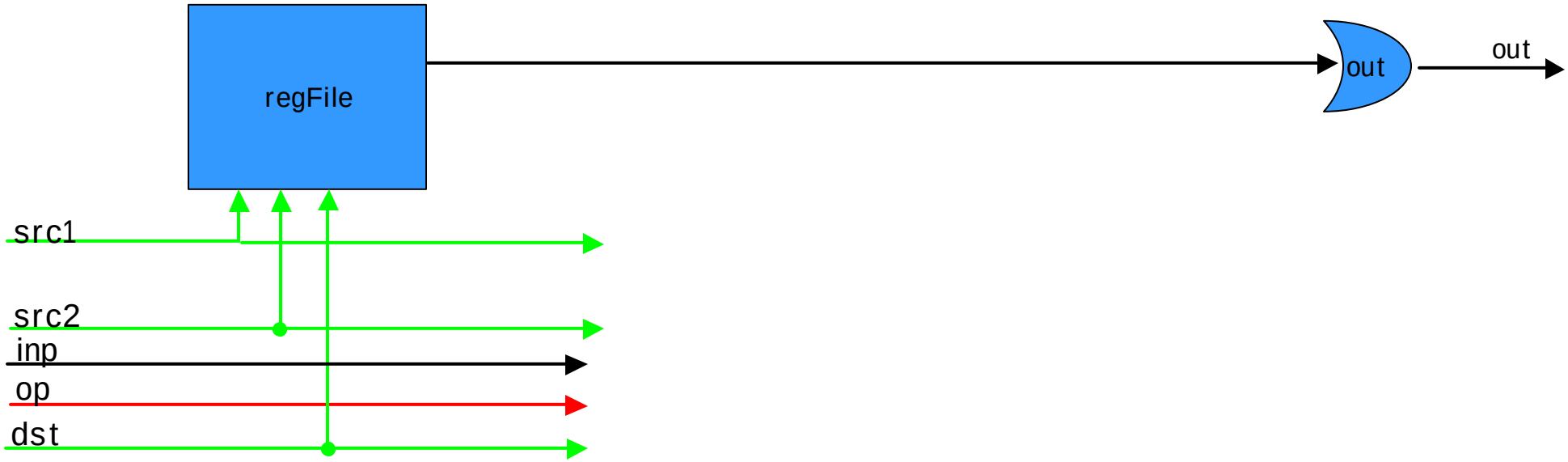
Why not decompose proof?

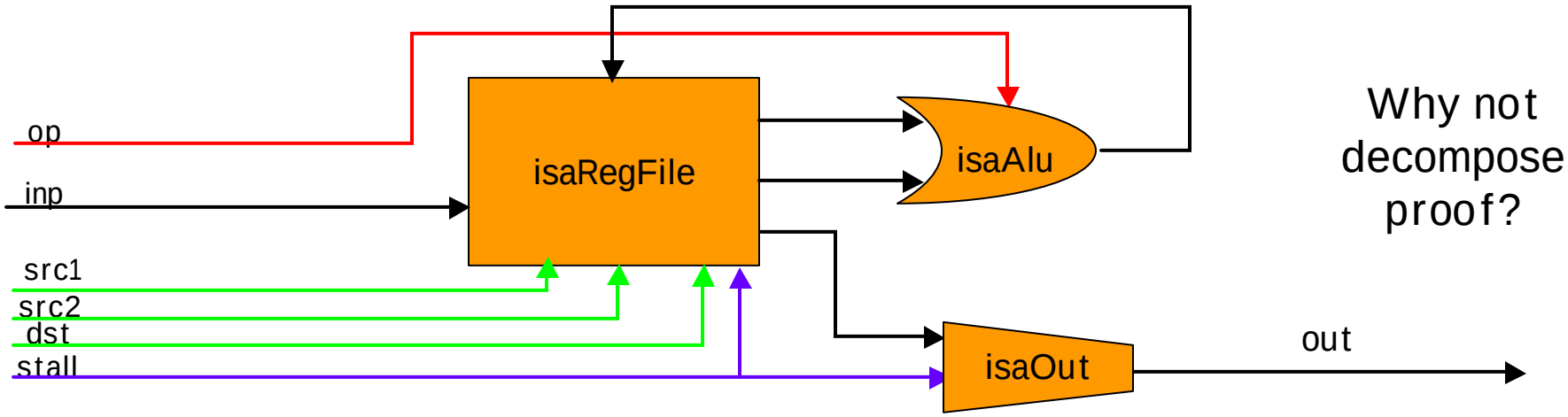






Why not decompose proof?





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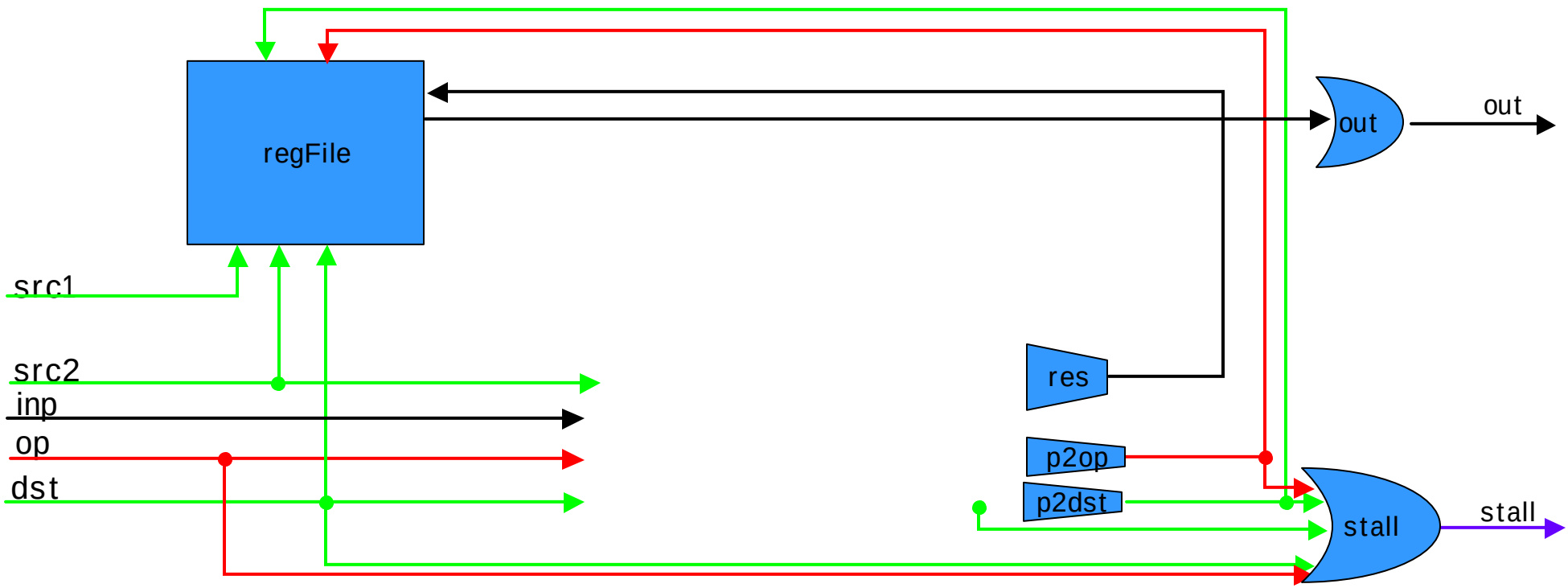

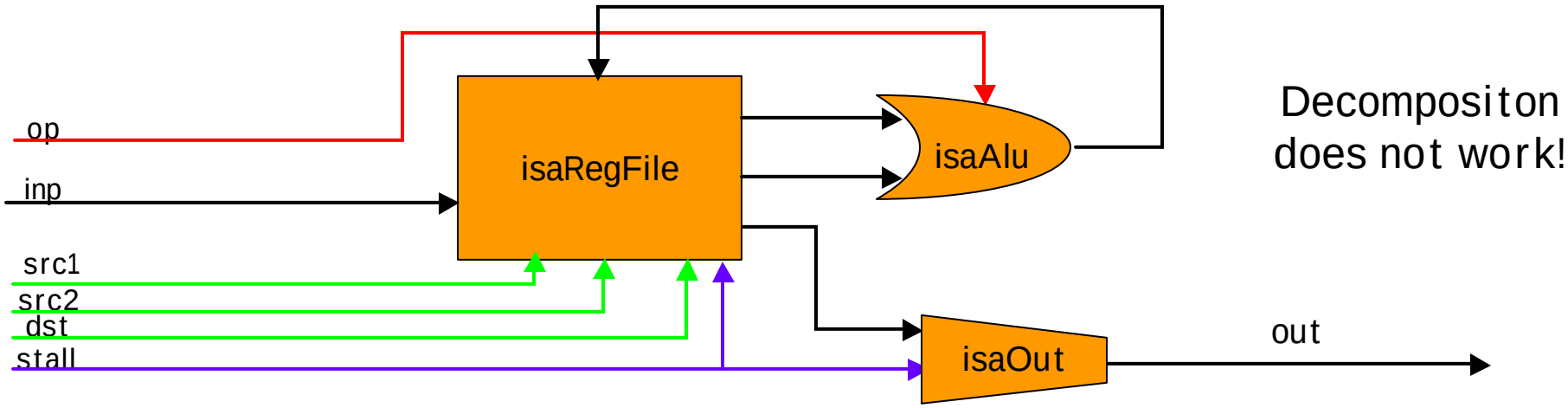
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isaAlu
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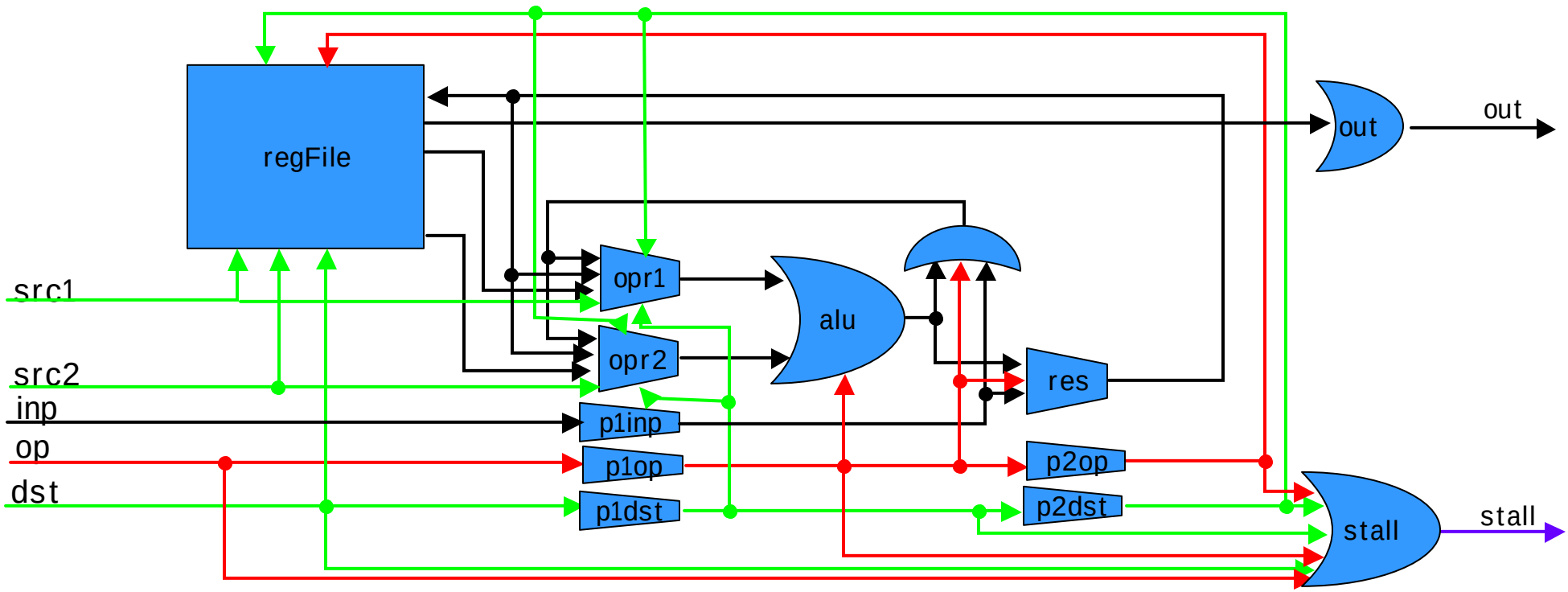
out
Decompositon
does not work!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alu
res
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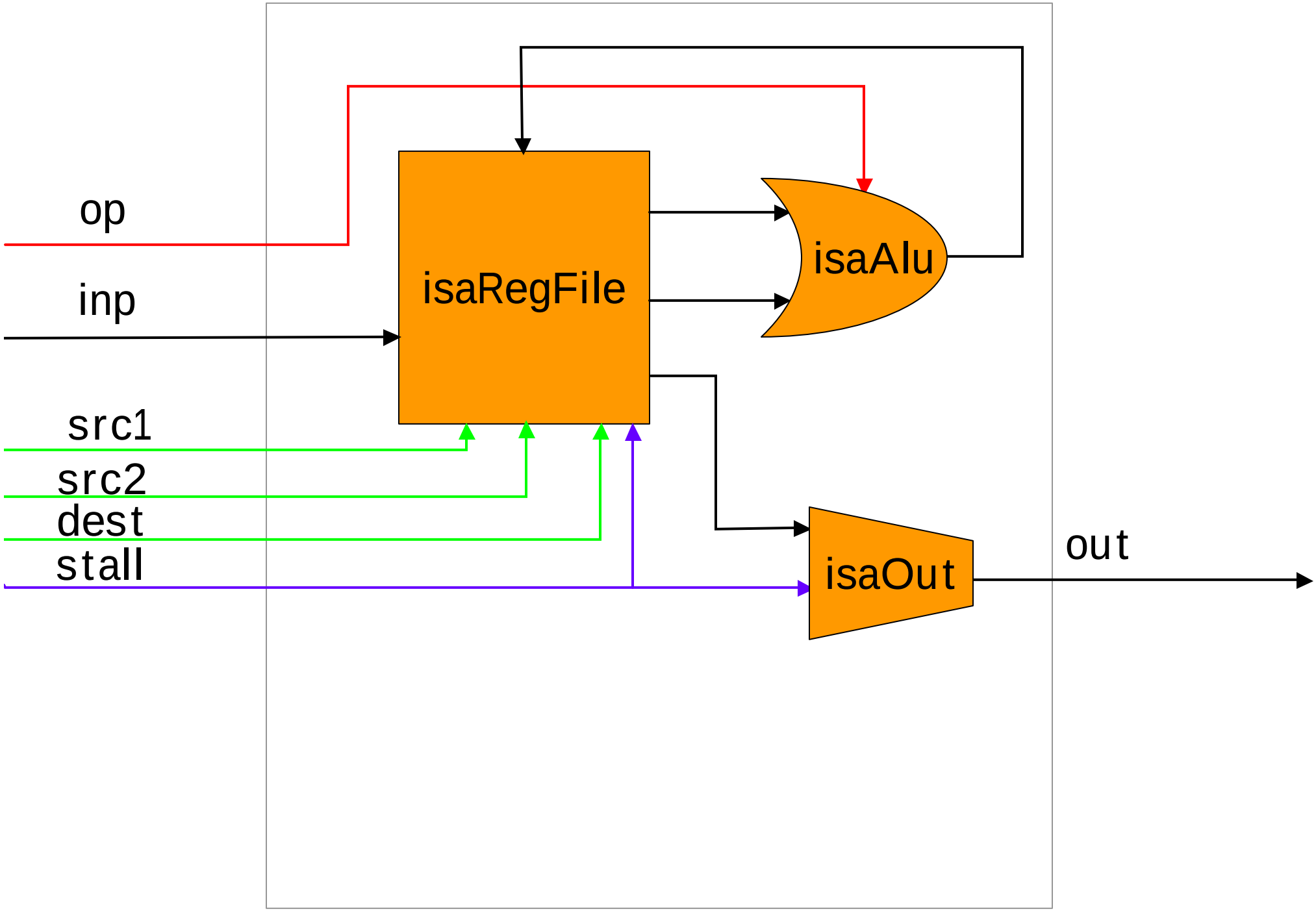
stall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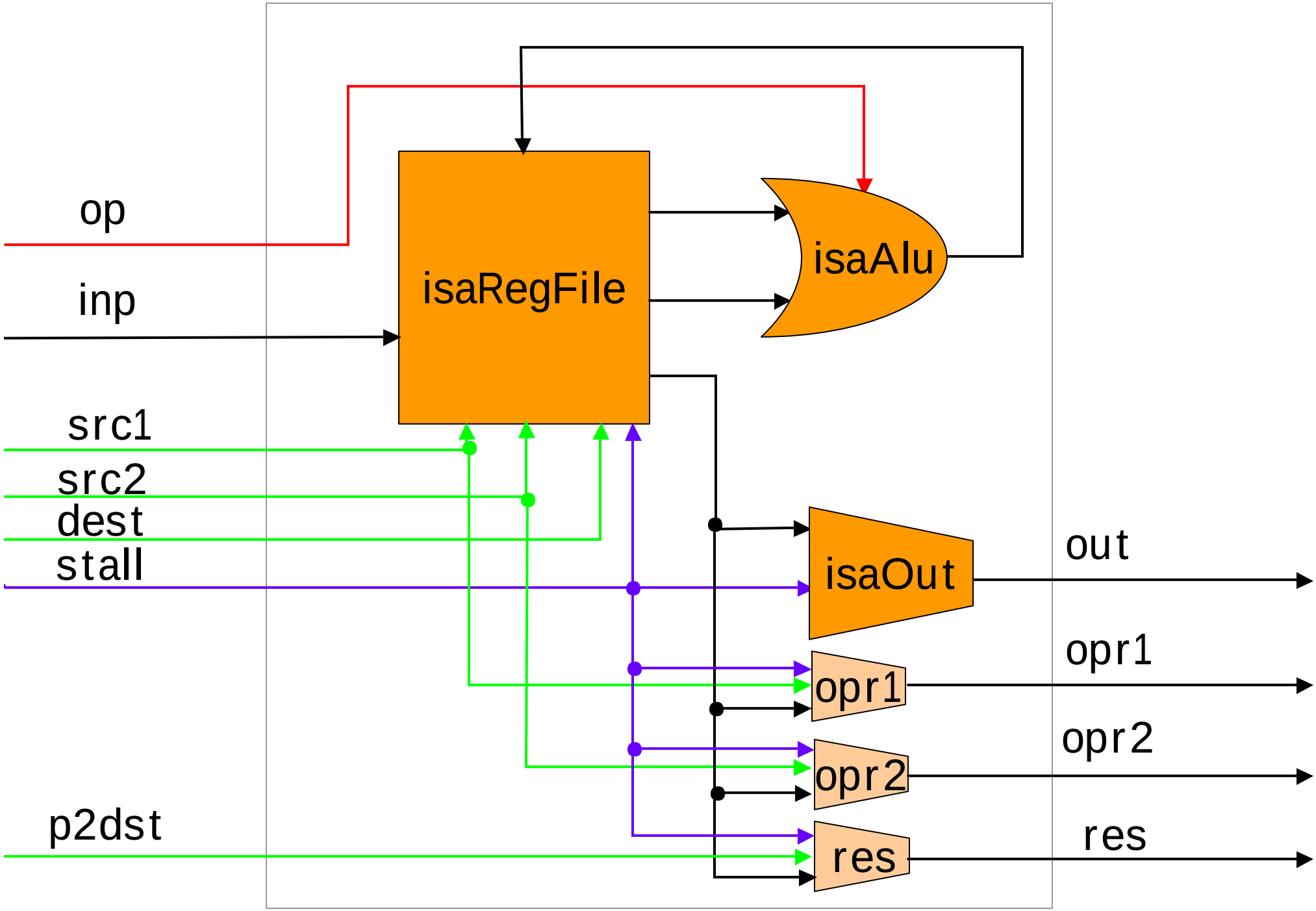
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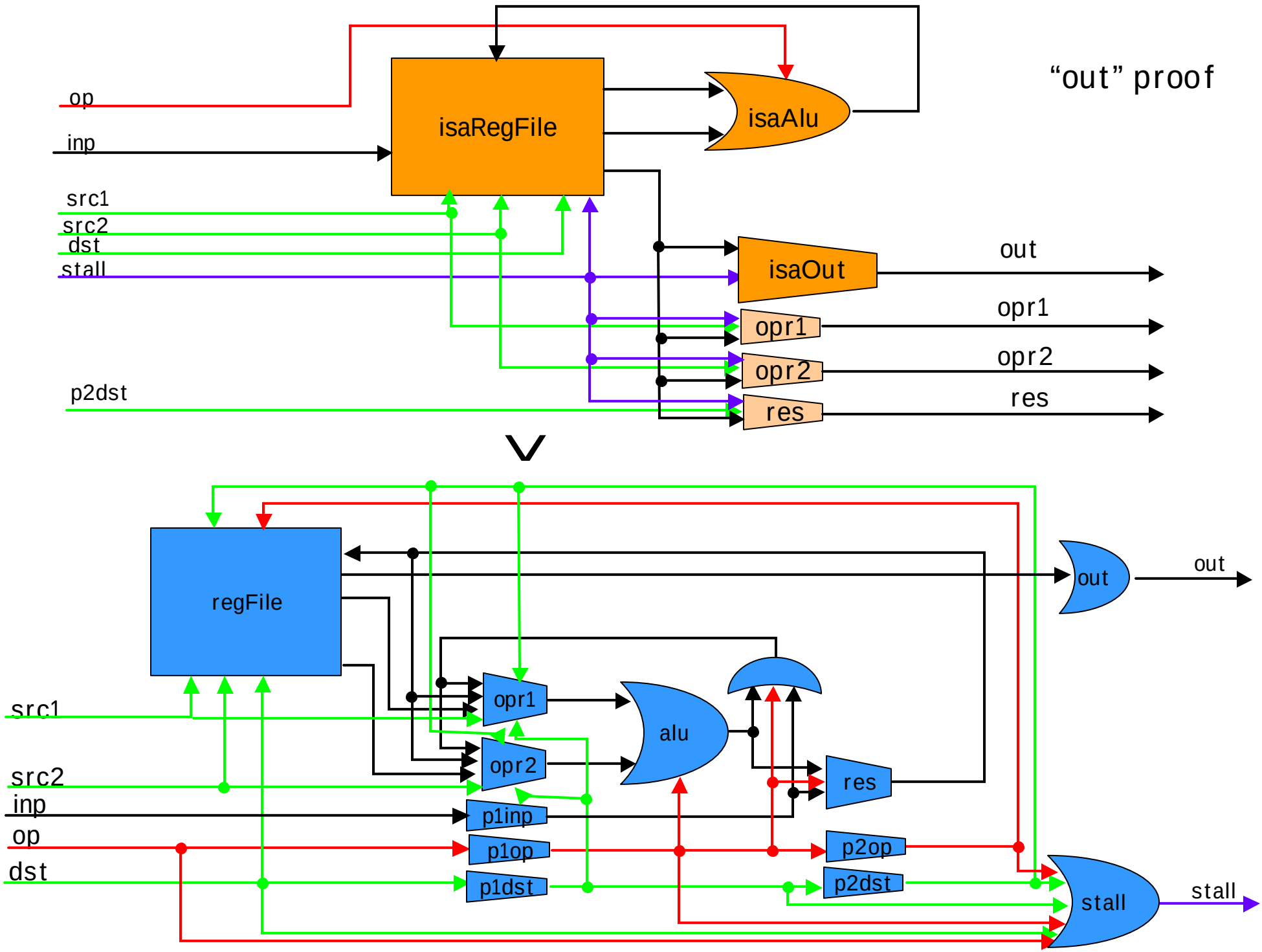
res


"out" proof
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p2dst
res
res
regFile
out
out
opr1
alu
src1
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p1op
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p1dst
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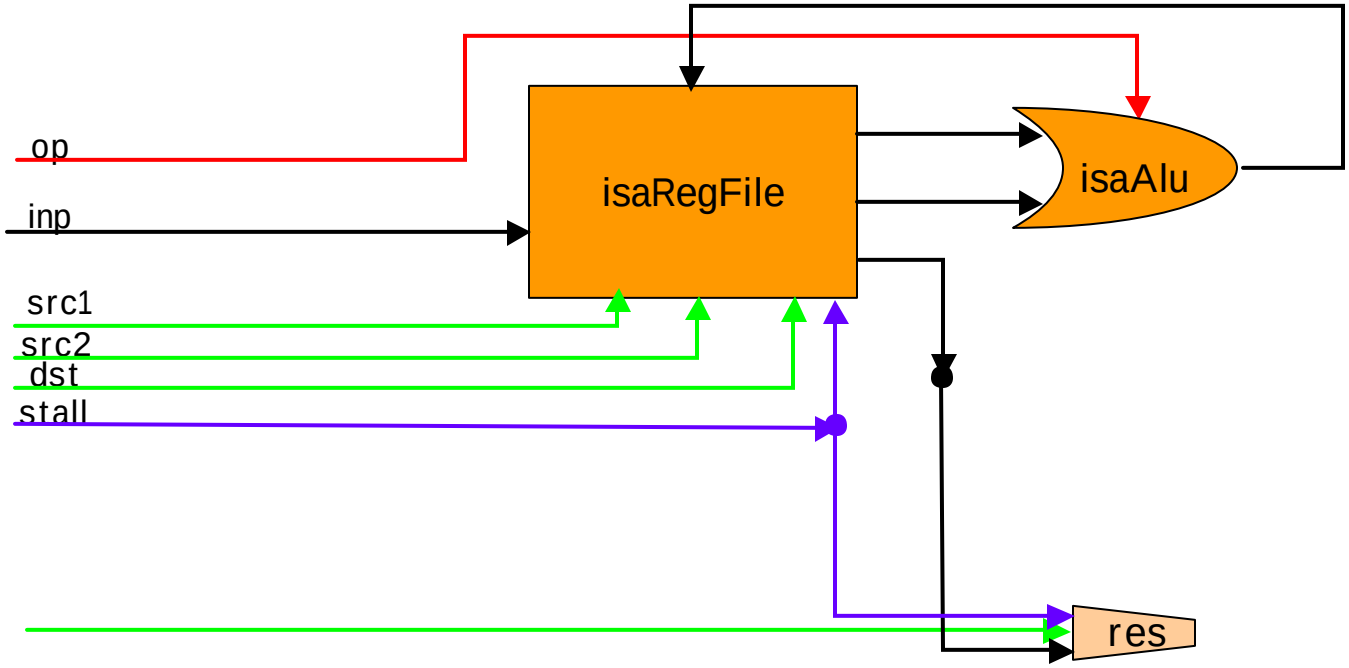
stall
stall

“out” proof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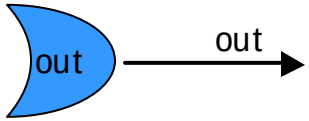
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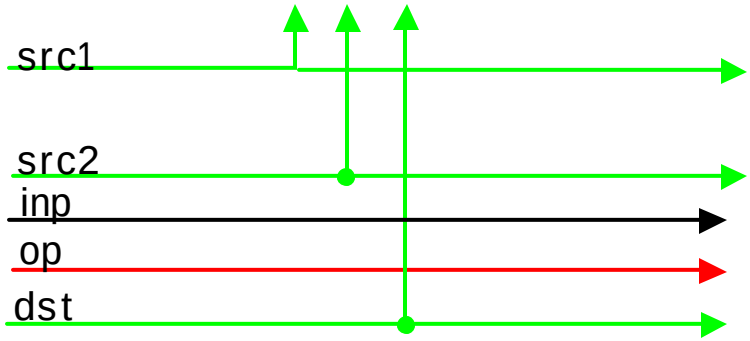
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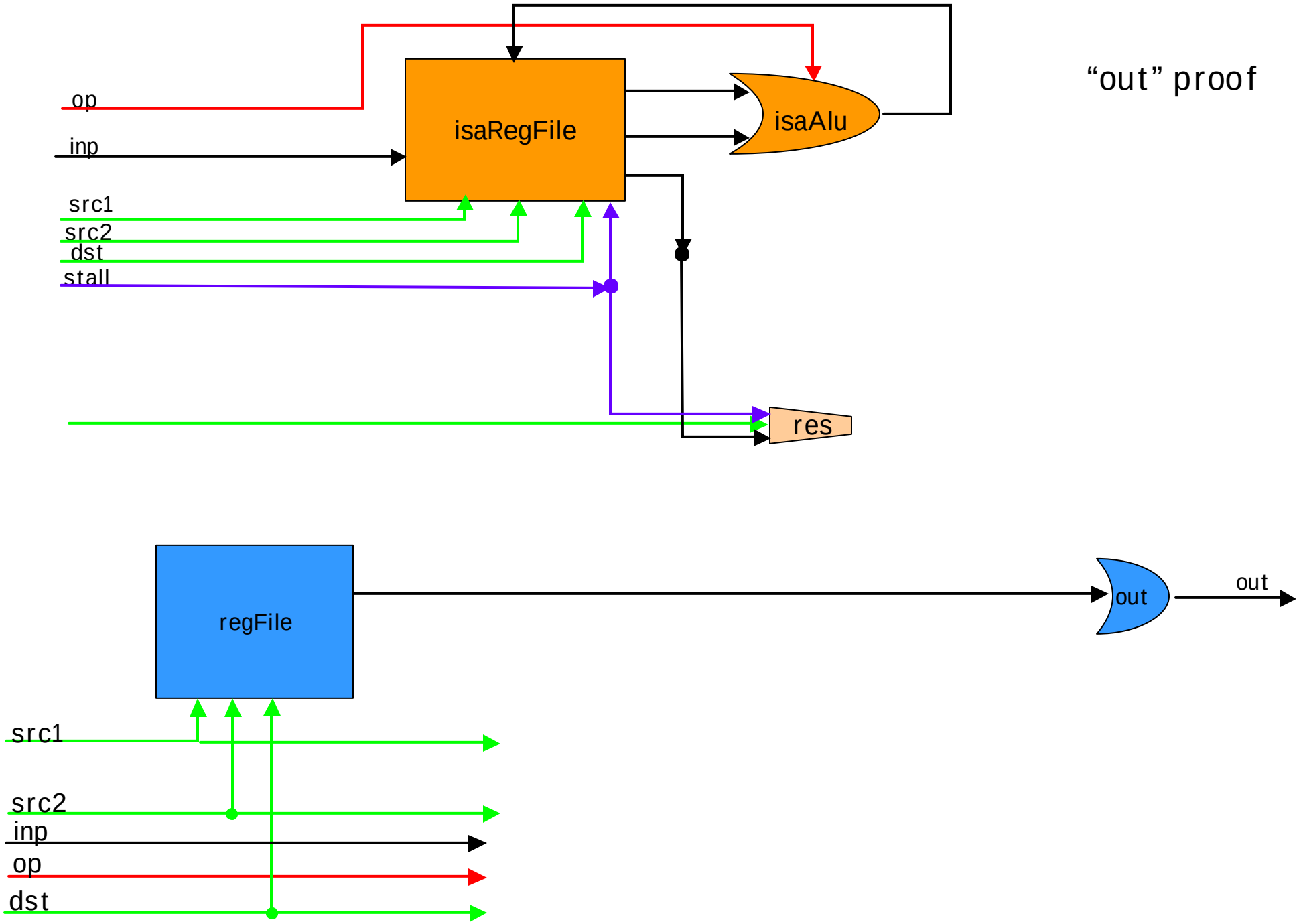
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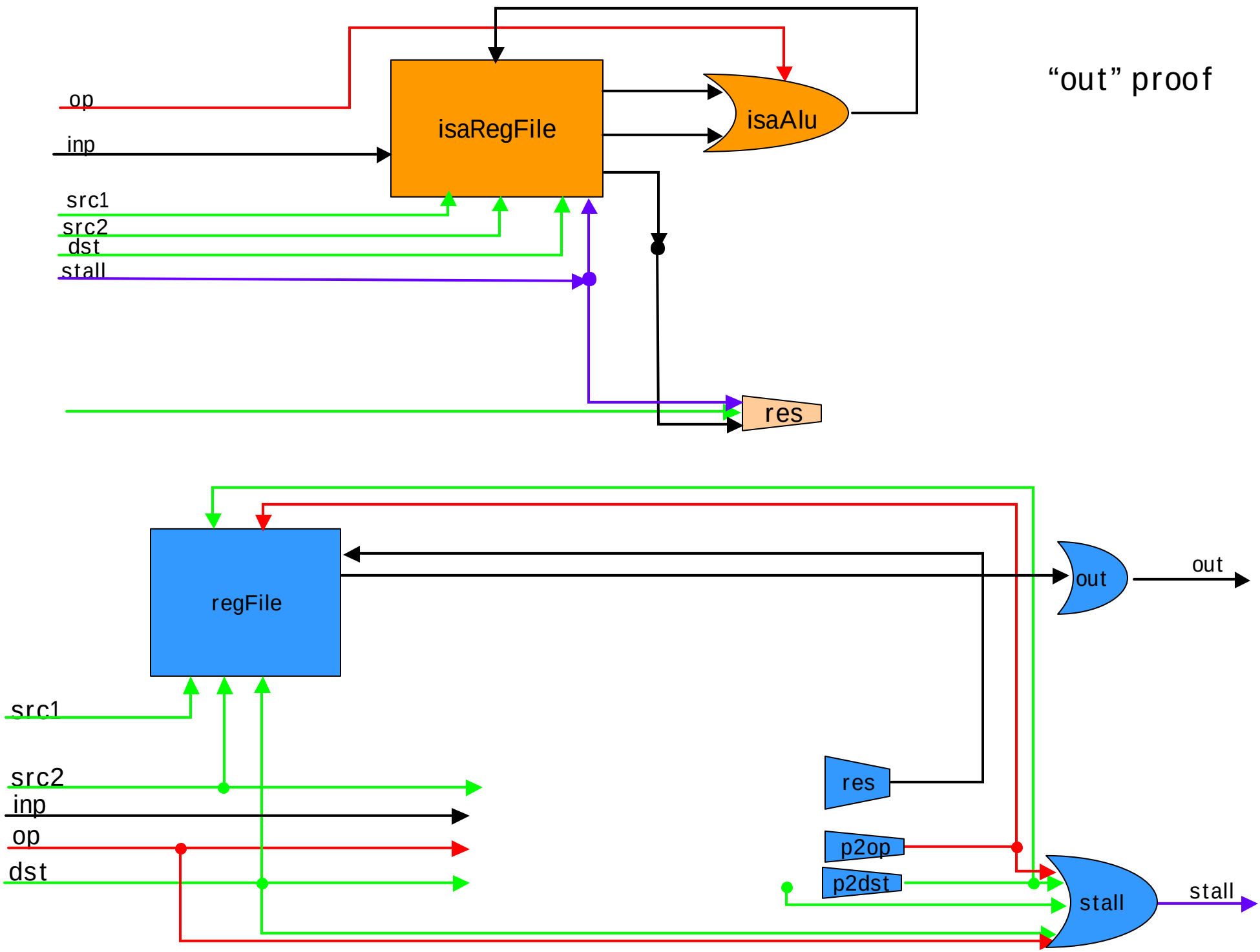
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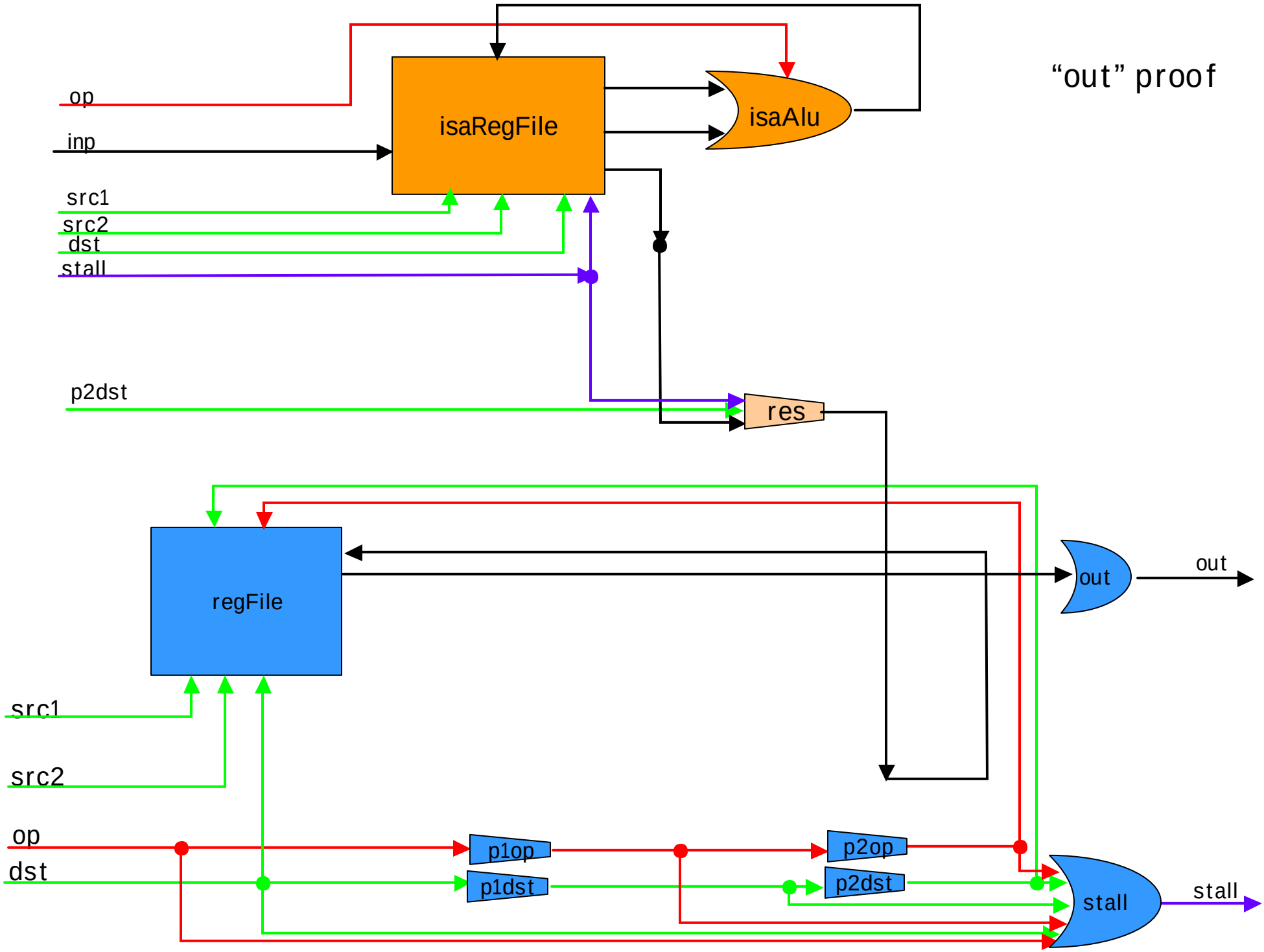
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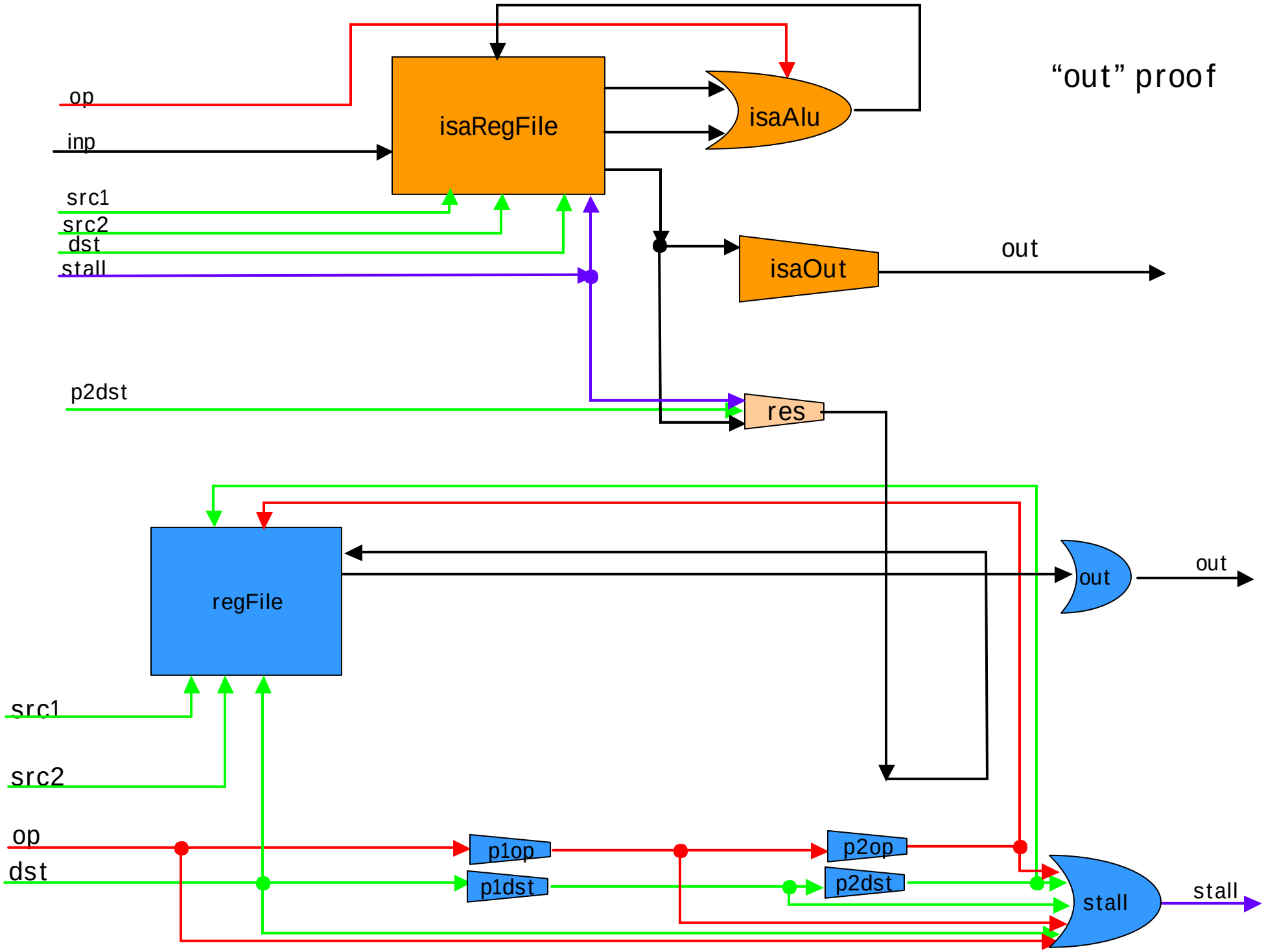
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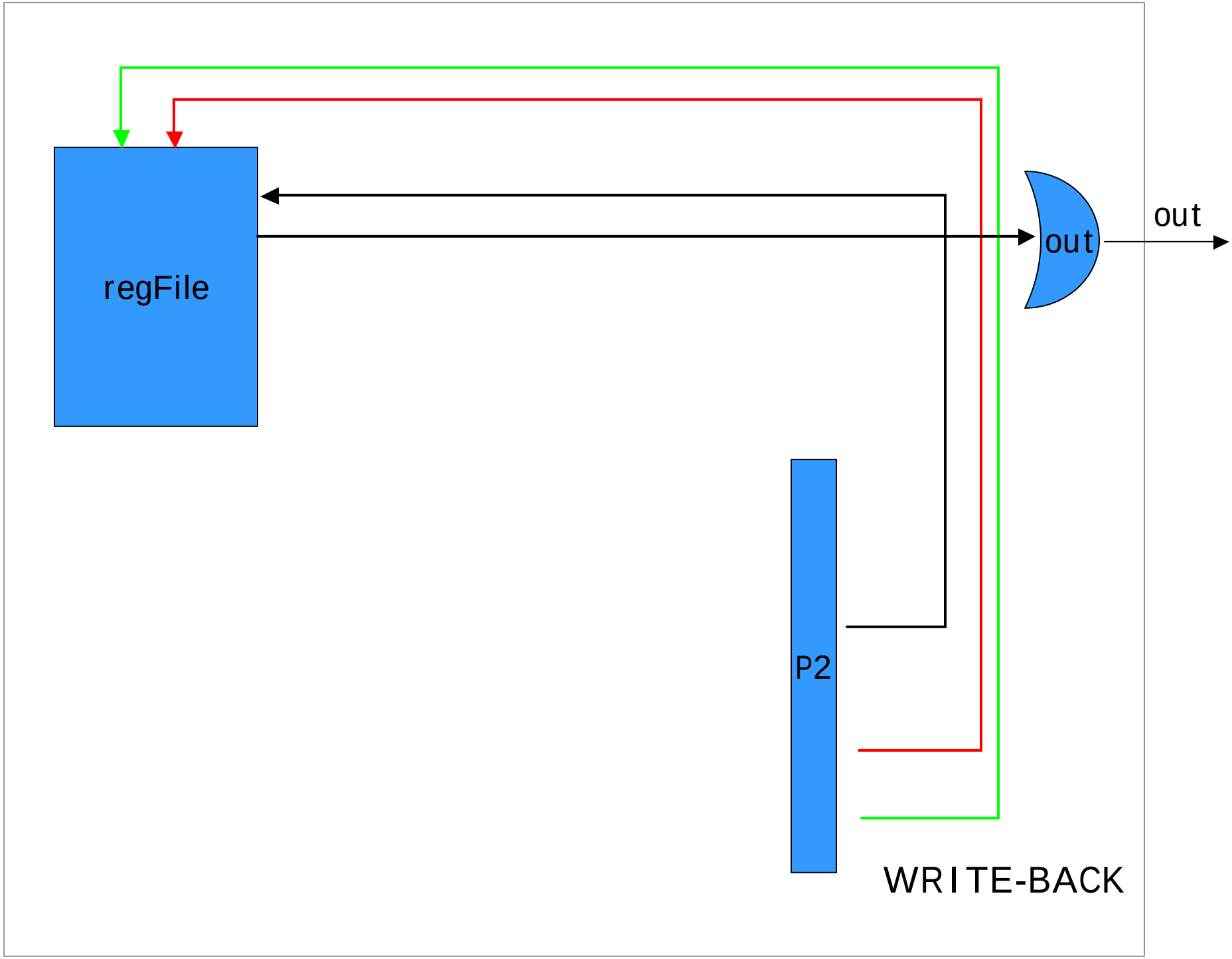
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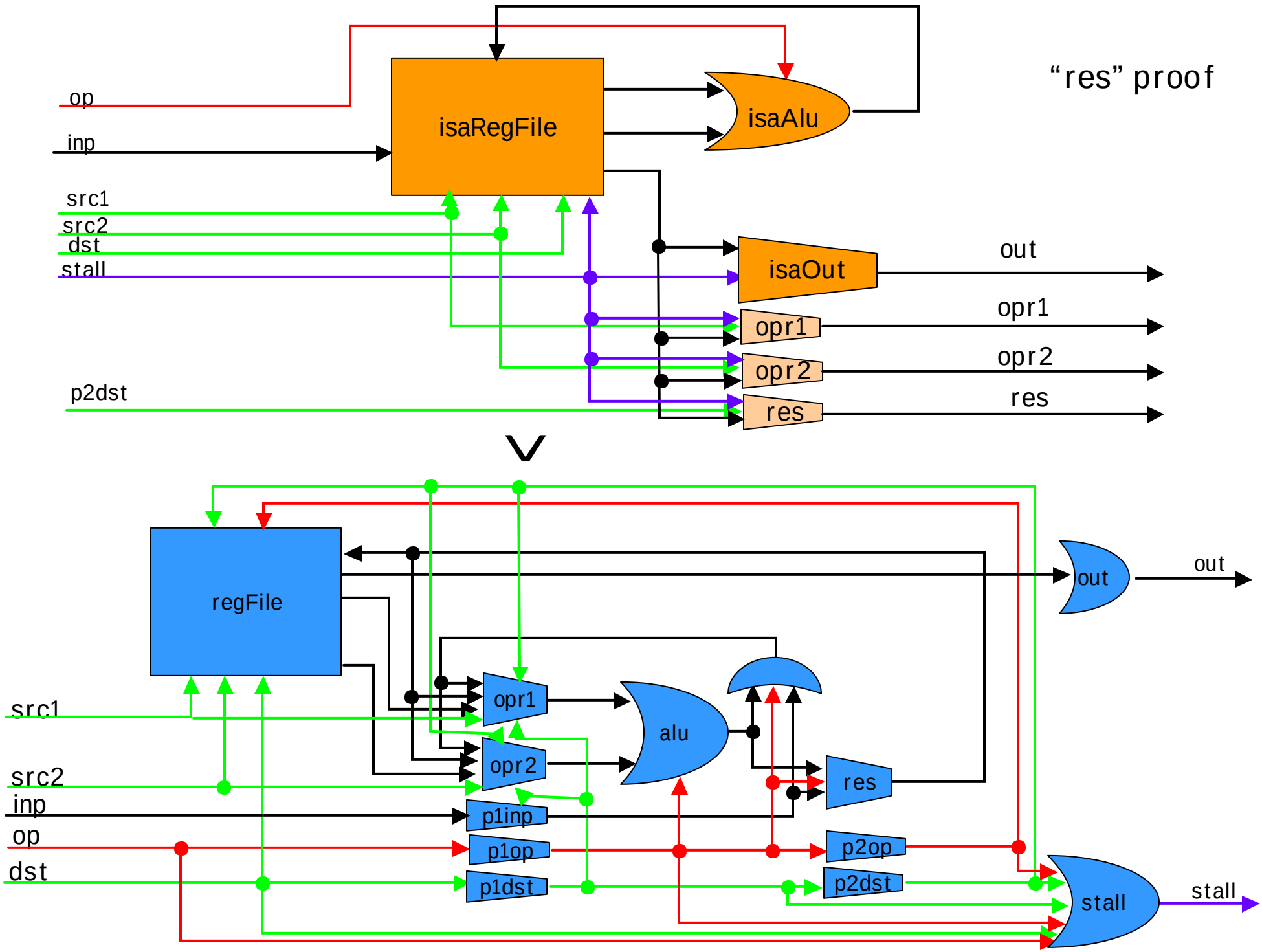
out
P2
WRITE-BACK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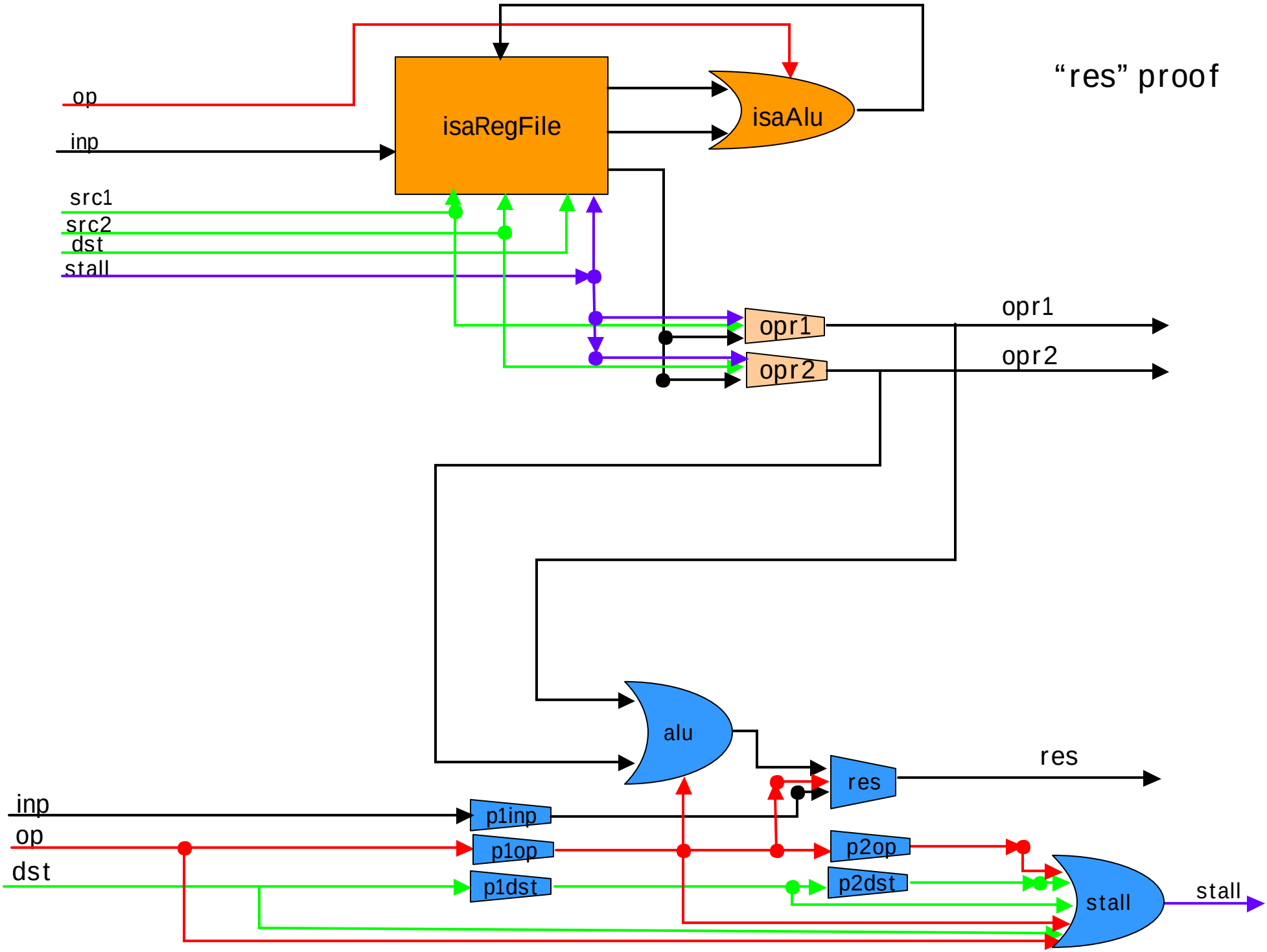
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opr1
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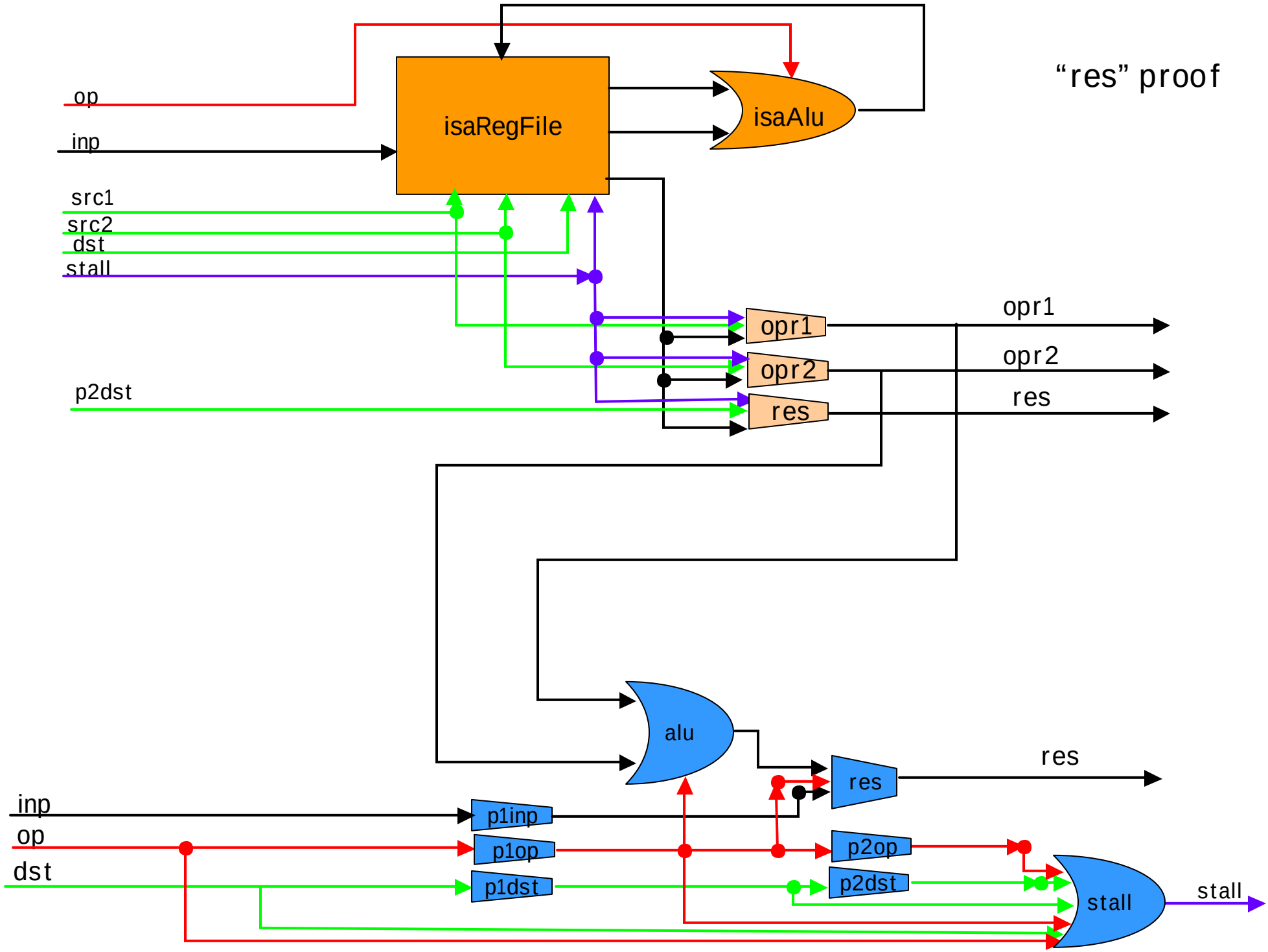
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inp
isaRegFile
isaAlu
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src2
dst
stall
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opr2
res
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opr2
res
alu
res
res
inp
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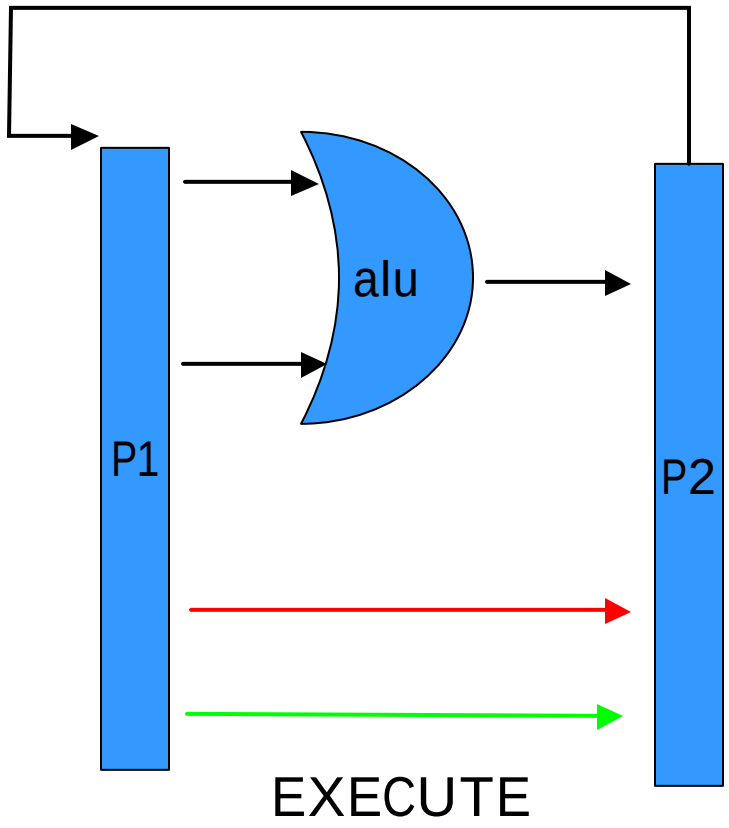
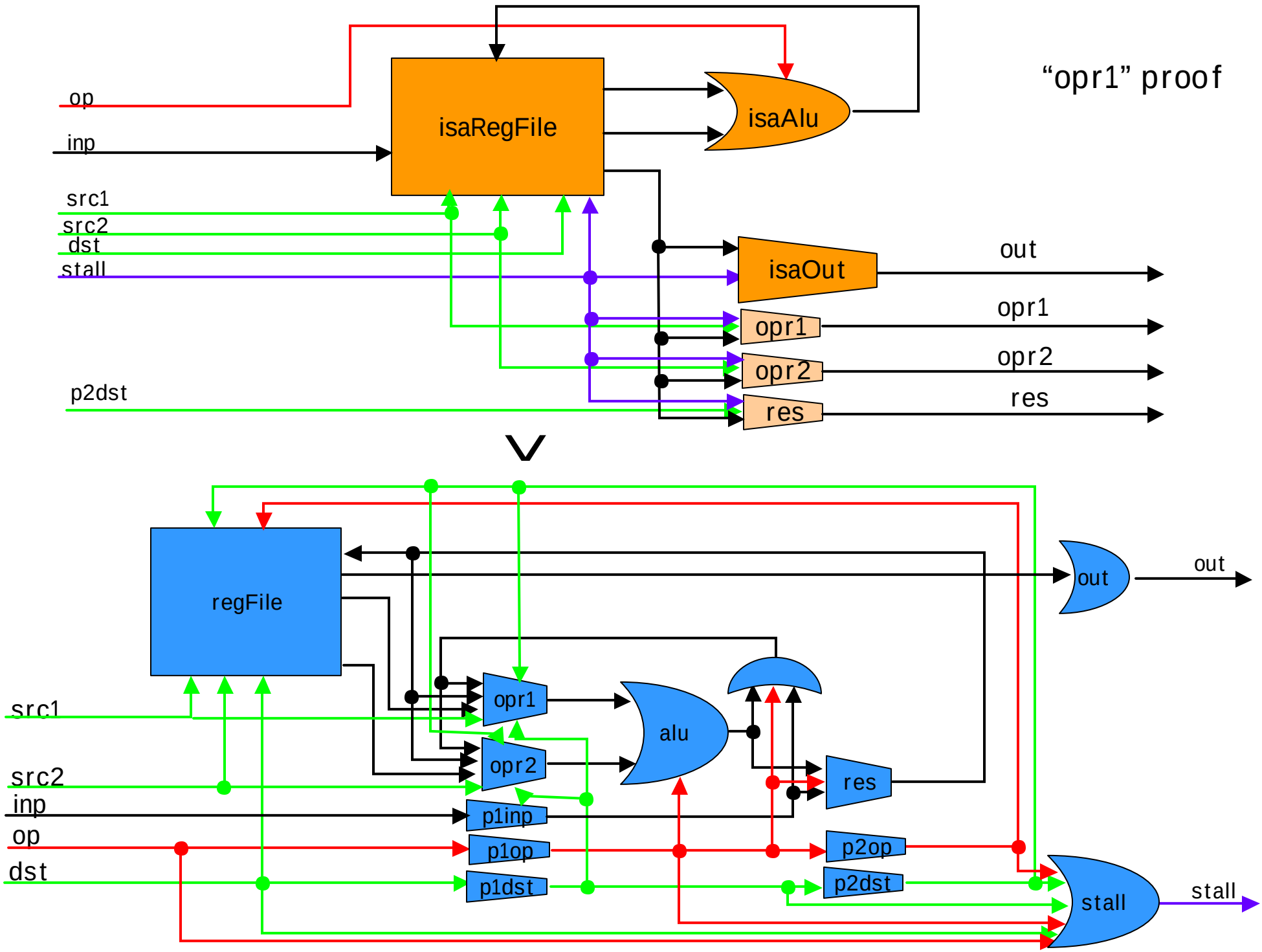
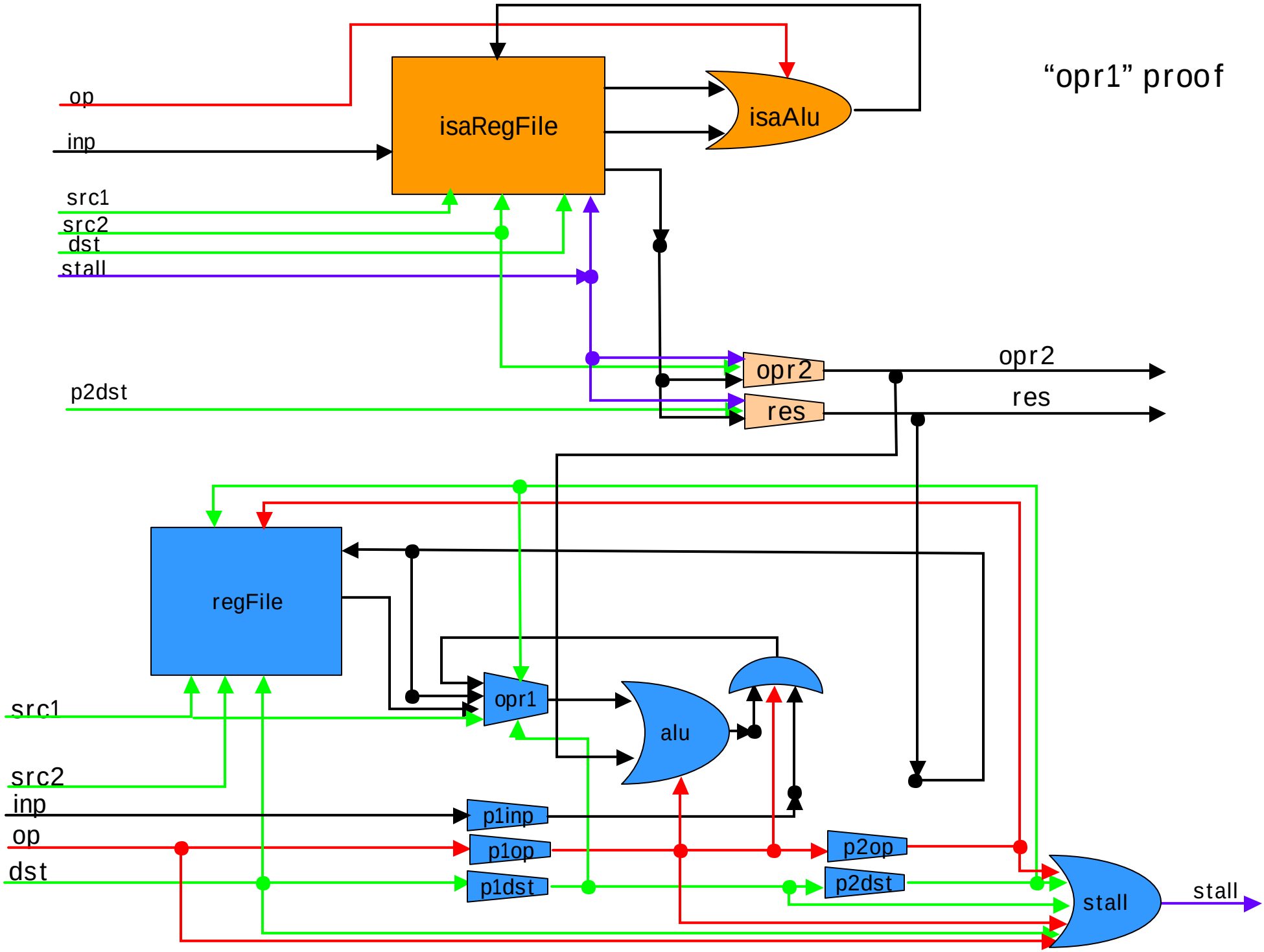
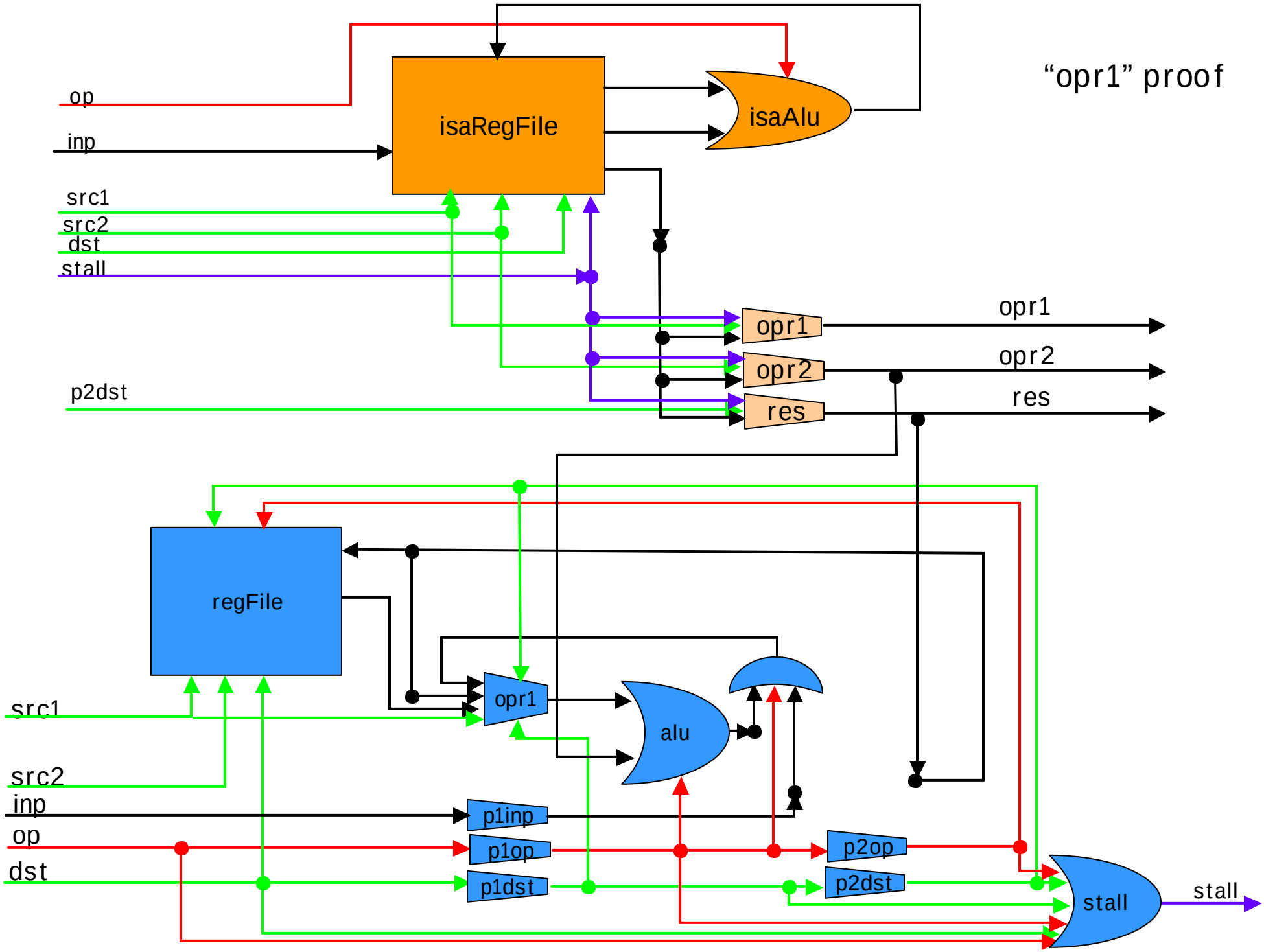
p1op
p1dst
p2op
p2dst
stall
stall


alu
P1
P2
EXECUTE


"opr1" proof
op
inp
isaRegFile
isaAlu
src1
src2
dst
stall
isaOut
out
opr1
opr2
res
p2dst
regFile
out
opr1
alu
opr2
res
p1inp
p1op
p1dst
p2op
p2dst
stall
stall


"opr1" proof
op
inp
isaRegFile
isaAlu
src1
src2
dst
stall
opr2
res
p2dst
opr2
res
regFile
opr1
alu
src1
src2
inp
op
dst
p1inp
p1op
p1dst
p2op
p2dst
stall
stall


"opr1" proof
op
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src1
src2
dst
stall
opr1
opr2
res
opr1
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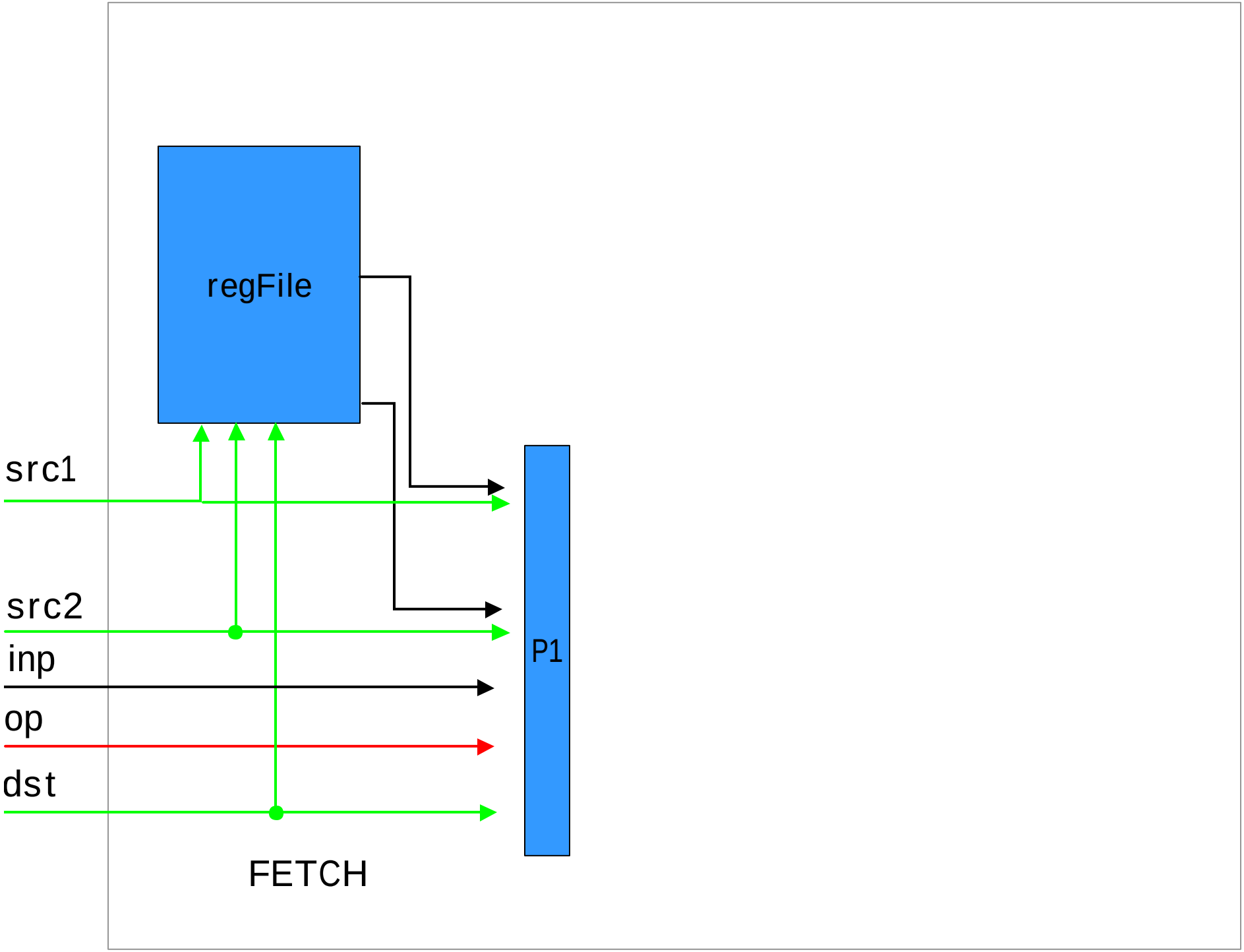
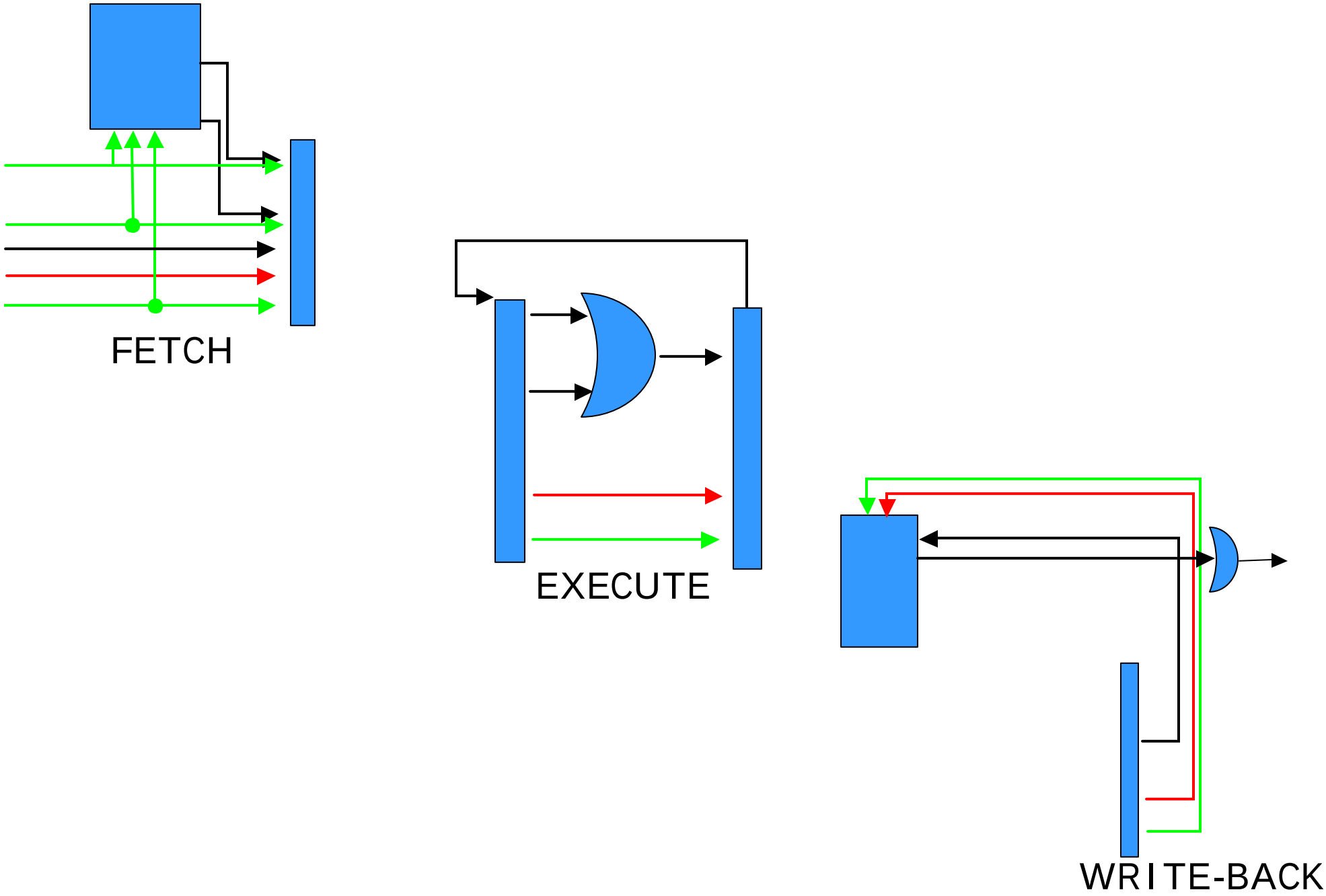
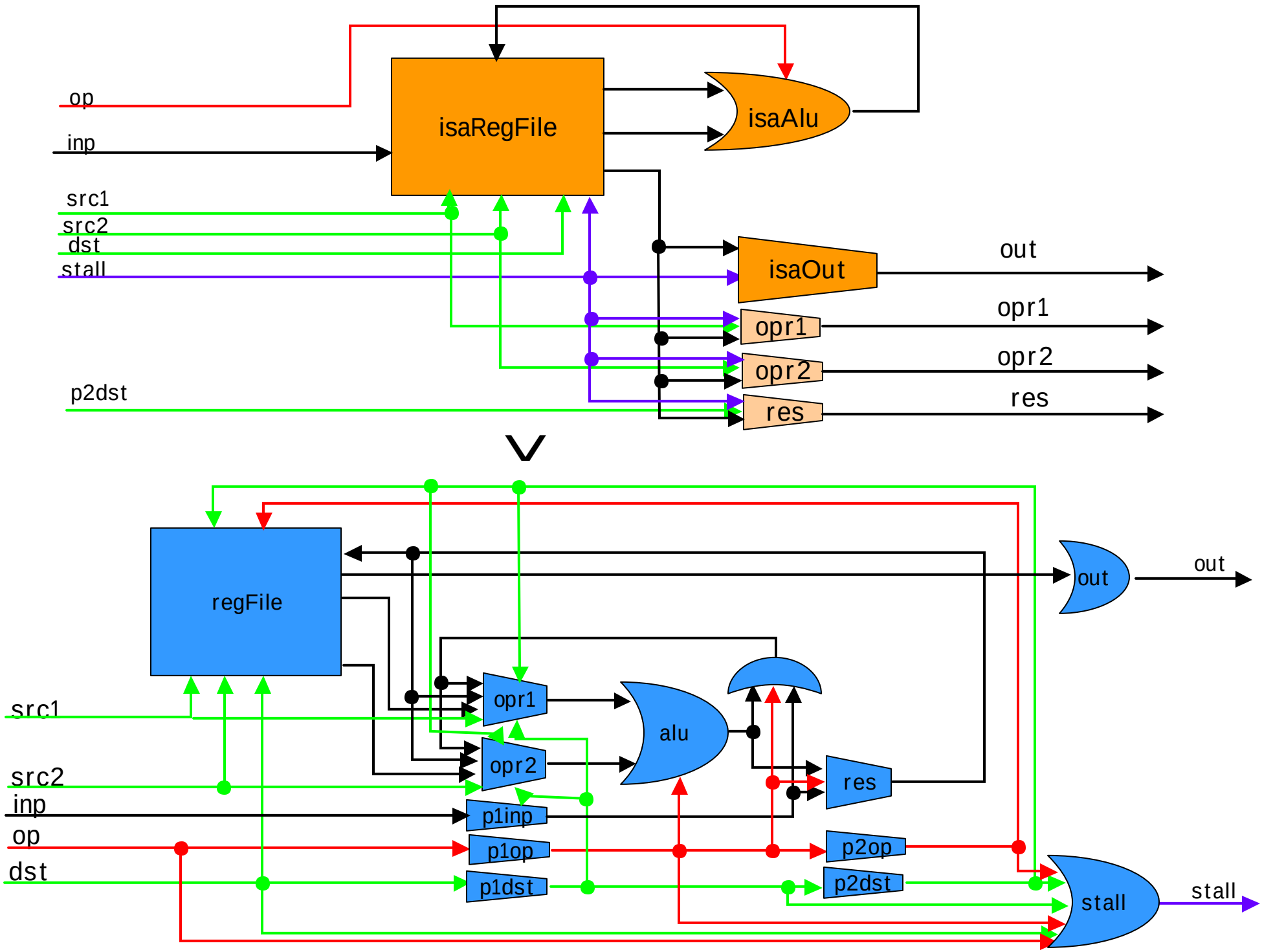
res
p2dst
regFile
opr1
alu
src1
src2
inp
op
dst
p1inp
p1op
p1dst
p2op
p2dst
stall
stall


regFile
src1
src2
inp
op
dst
P1
FETCH


FETCH
EXECUTE
WRITE-BACK


op
inp
isaRegFile
isaAlu
src1
src2
dst
stall
isaOut
out
opr1
opr1
opr2
opr2
p2dst
res
res
regFile
out
out
opr1
alu
opr2
res
src1
src2
inp
p1inp
op
p1op
p2op
dst
p1dst
p2dst
stall
stall

But… is this really practical?

Outline

1 Informal Introduction

2 Formal Definitions

- Reactive Systems
- Witnessed Refinement Proofs
- Slicing Reactive Systems
- Decomposing Refinement Proofs

3 Formal Example: Three-Stage Pipeline

4 Informal Example: Dataflow Processor Array

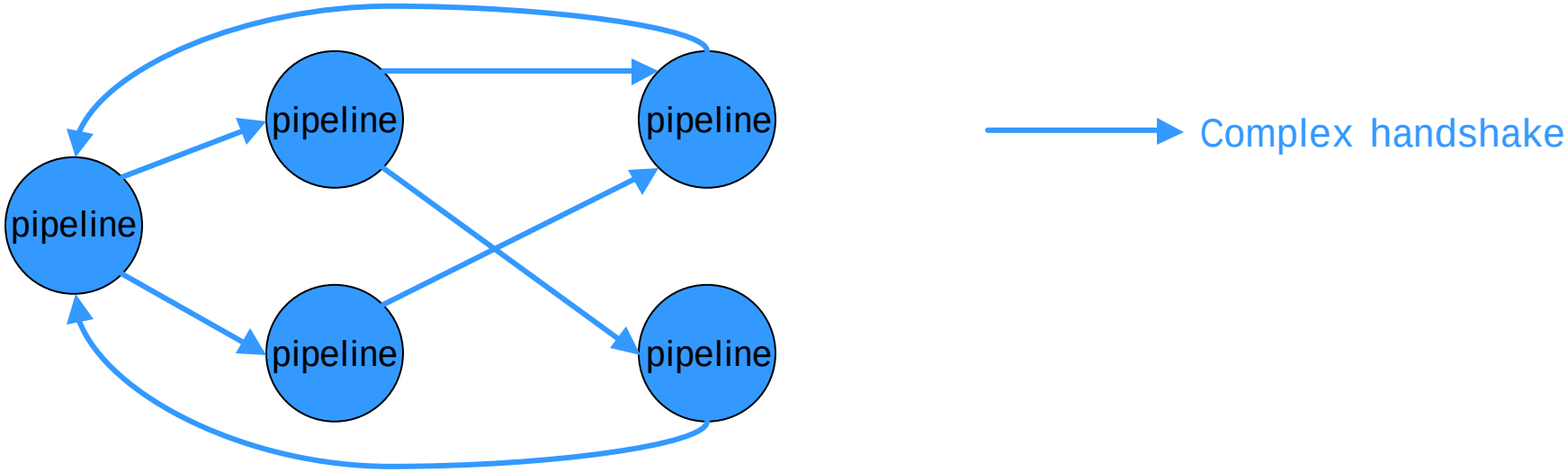
VGI Chip

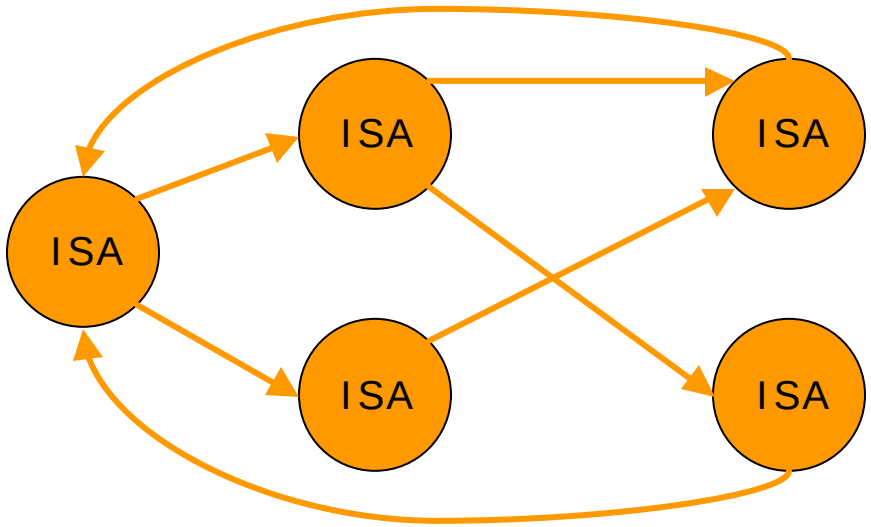
- VGI = “Video-Graphics-Image”
- Designed by Infopad group at Berkeley
- Purpose: web-based image processing
- Designed using
  - VHDL (control)
  - Schematics (data path)

VGI Architecture

- 16 clusters with 6 processors in each - 4 compute, 1 memory, 1 I/O
- ~30K logic gates per processor
- ~800 latches per processor
- Pipelined compute processors
- Low latency data transfer between processors - complex control

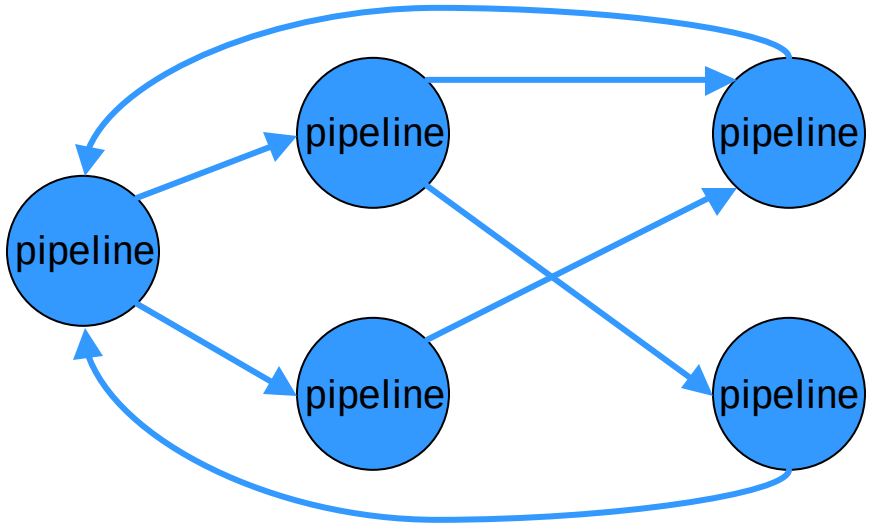
VGI Architecture





FIFO buffer

V



Complex handshake

Difficulties in Verification

Size of the VGI chip

- ~800 latches in each compute processor
- 64 compute processors
- Need two levels of “divide and conquer”

Different time scales

- Two-phase clk and level-sensitive latches in implementation
- Need special assume-guarantee rule

VGI Results

- All lemmas (exceptALU) checked by Mocha in a few minutes
- Three bugs in communication control found and fixed
- Abstract definitions crucial - designer insight needed

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