Computer-Aided Verification

Tool Lab Assignment (2)

Due Date: 2006/06/07

Bounded Model Checking

This tool lab aims at familiarizing yourself with bounded model checking and comparing its results with BDD-based model checking.

Download and install the latest version of the **NuSMV** tool from http://nusmv.irst.itc.it/.

Choose a system or component design that is **hard to verify using BDDs**, such as a multiplier unit.

Model the design using the input syntax of NuSMV. Inject a bug into your design, which can be found when the bound is **at least 3 clock cycles**. Specify an **LTL property** to detect the bug such that it is found when the bound is reached. Record the **counterexample** found from this bounded model checking process.

Verify the same design as above using **BDD-based model checking** in NuSMV and record the **counterexample** found.

Compare these two counterexamples and the time required for these two processes.

You must hand in your NuSMV program, the verification results (both counterexamples), and a single page containing a description of the comparisons you made.