Module 10
Basic VHDL (Version 2.05)

IV. BASIC VHDL Constructs Section Questions
(Insert link to these questions following page S00079)

10.IV.1. Which of the following statements about subtypes is false or inaccurate?

a) Subtypes are a constrained form of types
b) Subtypes define new types
c) SUBTYPE assignments out of the TYPE range are illegal
d) SUBTYPE negative IS integer RANGE –2147483647 to 1.

10.IV.2. Which of the following VHDL statements is an incorrect example of the specified data type?

a) An example use of subtype
```
TYPE all_numbers IS ( ’1’, ’12’, ’123’, ’1234’, ’12345’);
    SUBTYPE favorite_numbers IS all_numbers RANGE ‘12’ TO ‘12345’;
```
b) An example of access type
```
TYPE switch IS ACCESS switch_info;
```
c) An example of enumeration type
```
TYPE operations IS (ADD, SUB, MUL, DIV);
```
d) An example of array type
```
TYPE my_range IS RANGE 20 to 30;
```

10.IV.3. Which of the following is not a VHDL data object

a) signal
b) variable
c) wire
d) constant

10.IV.4. Which of the following statements is true?

a) constants, signals, and variables are data objects
b) enumeration, integer, physical and floating point are scalar types
c) arrays and record types are composite types
d) the key difference between variables and signals is the assignment delay

10.IV.5. Which of the following statements about objects is incorrect or inaccurate?

a) Objects declared in a package are available to all VHDL descriptions that *use* that package
b) Objects declared in an entity are available to all architectures associated with that entity
c) Objects declared in an architecture body are available to all statements in that architecture
d) Objects declared in a process are available to all processes in the architecture body

10.IV.6. Which of the following is not a correct or accurate statement about constants?

a) CONSTANT perfect_score: NATURAL := 100;
   is an example of a constant declaration
b) The assignment of the value to a constant can be done in a package
c) The value of a constant must be assigned at the time the constant is declared
d) The declaration of a constant can appear in a process

10.IV.7. Which of the following VHDL Objects provides a convenient mechanism for local storage by limiting scope to the process where they are declared.

a) signals
b) variables
c) constants
d) files

10.IV.8. VHDL objects of the _____ class are analogous to wires in a design schematic. They have a history of past, present and future values and their assignment is done after a certain delay.

a) signals
b) variables
c) constants
d) files

10.IV.9. VHDL _____ objects are used for text input and output, and provide a way for the design to communicate with the host environment.

a) signal
b) variable
c) file
d) constant

10.IV.10. Which of the following statements are true?

a) All VHDL processes execute concurrently
b) Concurrent signal assignment statements are one-line processes

c) Statements in a process execute sequentially
d) All of the above

10.IV.11. Which of the following statements are true?

a) Packages and libraries provide the ability to reuse constructs in multiple entities and architectures
b) Items declared in packages can be *used* (i.e. included) in other VHDL components
c) Packages consist of two parts, namely the package declaration and the package body
d) All of the above

10.IV.12. The following fragment of VHDL code illustrates the use of what construct?

```
IF clock'event AND clock = '1' THEN
        output <= input +1
END IF;
```

a) attributes
b) clocks
c) comments
d) identifiers

10.IV.13 Logical operators have _____ compared to other operators

a) lowest precedence
b) highest precedence
c) medium precedence
d) no precedence

10.IV.14. Which of the following is an incorrect VHDL enumerated data type declaration

a) TYPE weather_condition IS (good, sunny, cloudy, rainy, storm);
b) TYPE currency IS (dollar, quarter, dime, nickel, penny)
c) SUBTYPE my_currency IS currency RANGE quarter TO nickel;
d) TYPE peripherals IS (monitor, keyboard, disk_drive, printer);
e) none of the above

10.IV.15. Which of the following is a correct VHDL integer type declaration?

a) CONSTANT temp : integer := 100;
b) SIGNAL x : integer := 5;
c) VARIABLE var : integer := 20;
d) All of the above

10.IV.16. The VHDL Record composite data type is used to group elements of _____ types into a single VHDL object.

a) similar
b) different
c) identical
d) integer
e) floating point