Module 10
Basic VHDL

III. Model Components Section Questions
(The slides for these questions start at Slide 44.)

10.III.1. Which of the following is the most accurate statement about VHDL entities and architectures?

a) A component can have many entity declarations and many architectures.
b) A component can have many entity declarations but only one architecture.
c) A component can have only one entity declaration and many alternative architectures.
d) A component can have only one entity declaration and only one architecture.

10.III.2. Which VHDL statement is used to create parameters which are passed on to the architectures of an entity?

a) generate statement
b) generic statement
c) guard expression
d) globally static-expression

10.III.3. Logic gates may have a minimum input pulse width specification (whereby shorter input pulses are not reproduced at the output). If a VHDL model must duplicate this logic behavior, then which of the following delay models should be used?

a) inertial delay model
b) transport delay model
c) delta delay model
d) any one would produce the desired result

10.III.4. Which of the following delay models should be used to simulate just the effect of logic propagation delays.

a) inertial delay model
b) transport delay model
c) delta delay model
d) any one of them would serve the purpose

10.III.5. Which of the following statements accurately describe “delta delay”?

a) It is an infinitesimal VHDL time unit.
b) It is used so that all signal assignments can result in signals assuming their values at a future time.
c) It is the default signal assignment if no explicit delay model is used

d) All of the above