Module 10
Basic VHDL

II. Design Example Section Questions
(The slides for these questions start at Slide 26.)

10.II.1. A VHDL Model which instantiates components and then interconnects them with each other (and with the outside world) by attaching signals using PORT MAPS most likely represents which of the following styles of VHDL model?

a) Behavioral Specification
b) Data Flow Specification
c) Structural Specification

10.II.2. A VHDL Model which uses abstracts constructs (such as If-Then-Else) most likely represents which of the following styles of VHDL model?

a) Behavioral Specification
b) Data Flow Specification
c) Structural Specification

10.II.3. A VHDL Model that exclusively uses concurrent signal assignment statements to describe the functionality of the design most likely represents which of the following styles of VHDL model?

a) Behavioral Specification
b) Data Flow Specification
c) Structural Specification

10.II.4. The time required to perform hardware simulation is directly proportional to the level of hardware fidelity in the model. That is, detailed models of physical hardware take much longer to simulate than abstract or algorithmic models. Which of the following VHDL modeling styles will result in the shortest simulation times?

a) Structural model
b) Dataflow (RTL) model
c) Behavioral model

10.II.5. Which style of VHDL Model is most appropriate for use during the early stages of a design?

a) Structural model (because components can be easily added and removed)
b) Dataflow (RTL) model (because logic equations can be easily manipulated for design modifications)
c) Behavioral model (because it is implementation independent)
d) Mixture of all three methods (because the appropriate level of abstraction can be chosen which is best suited for our design)