Module 10
Basic VHDL (Version 2.05)

V. VHDL Examples Section Questions
(Insert link to these questions following page S00089)

10.V.1. With reference to the VHDL code segment, which of the following statements is most accurate?

```
ARCHITECTURE test_behav OF test IS

VARIABLE  x : BIT := '1' ;

BEGIN
        PROCESS ( in_sig, y)
        SIGNAL y : BIT := '0';
        BEGIN

                X := in_sig XOR y;
                Y <= in_sig XOR x ;
         END PROCESS;
END test_behav;
```

a) A variable (x) is incorrectly declared in the process declaration section
b) A signal (y) is incorrectly defined in the architecture declaration section
c) Both the Variable and Signal declarations are incorrect.
d) The code segment is error free

10.V.2. Fill in the blank line identified in the VHDL code fragment below with the appropriate command that will assign a value of one to the variable temp.

```
ARCHITECTURE test OF test IS
SIGNAL temp2: INTEGER;

BEGIN
PROCESS (temp2)
        VARIABLE temp: INTEGER;
BEGIN
        Fill in the blank here
        temp2 <= temp + 1;
        out <= temp2;
END PROCESS;
END TEST;
```

a) temp := '1';
b) temp := 1;
c) temp := 1.0 ;

d) temp := " 1 ";

10.V.3. Which of the statements below most accurately identifies the error(s) in the following VHDL code fragment?

```
ARCHITECTURE  test_enum OF test  IS
TYPE  state_type  IS (IDLE, START, CANCEL);

SIGNAL state : state_type
BEGIN
        PROCESS (state)
                VARIABLE next_state_value : STATE_TYPE;
        BEGIN
                        Next_state_value:= IDLE;
        CASE state IS
                WHEN IDLE =>
                        -- execute some ‘idle’ statements
                WHEN START =>
                        -- execute some ‘start’ statements
                WHEN CANCEL =>
                        -- execute some ‘cancel’ statements
                WHEN DONE =>
                        -- execute some ‘done’ statements
        END CASE;
        END PROCESS;
END test_enum;
```

a) All the objects declared are incorrectly specified as enumeration data types
b) The case statement includes the state DONE, which is not contained in the original enumerated type definition.
c) There is a semicolon missing at the end of the line: PROCESS (state)
d) There are no errors in the code

10.V.4. Which of the following statements most accurately identifies any errors in the VHDL Code fragment below?

```
ENTITY test is
        PORT (a, b: IN BIT; y, z: OUT BIT; clock: INOUT BIT);
END test;

ARCHITECTURE example OF test IS
   BEGIN
        a <= y AND z AND clock;
        b <= y NOR z AND clock;
        Clock <= NOT clock;
END example;
```

a) Signals y and z are incorrectly used as inputs within the architecture
b) Signals a and b are incorrectly assigned values within the architecture
c) Both (a) and (b)
d) Code is error free.