

A 90 nm All-digital Smart Temperature Sensor with Wireless Body Area Network Baseband Transceiver for Biotelemetry Applications

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Abstract This work provides an all-digital smart temperature sensor with dual-mode transceiver chipset for wireless body area network (WBAN). The measurement results show that the proposed temperature sensor achieves a maximum temperature error $<0.6^{\circ}\text{C}$ within the range from 20°C to 50°C . And a phase-frequency tunable clock generator (PFTCG) is designed with frequency and phase tuning capability on the fly. This chip is manufactured on a standard 90 nm CMOS process. The supply voltage to the chip core is globally applied at 0.5 V with 12 power-domain partitions for sleep-active and voltage-scaling management. The transceiver chipset provides maximum 7 Mbps data rate, resulting in 97.7% efficiency improvement in baseband circuit processing.

Keywords PLL · Temperature sensor · Power domain · Voltage scaling · WBAN

1 Introduction

Ubiquitous healthcare monitoring plays a crucial role in physical status tracking and recording. This extends medical services from the closed in-hospital systems to any open roaming spaces. Wireless body area network

(WBAN), consisting of a multiple wireless sensor nodes (WSNs) and a central processing node (CPN) [1], is specifically designed for bio-signal acquisition and monitoring to provide reliable physical information. The WSN is capable of sensing and processing body information, and transmitting the data wirelessly to a CPN. The WBAN, especially the WSN, is required to provide reliable signal exchanges with ultra-low power and highly integrated tiny chip area.

WBAN-oriented applications may cover from non-invasive to implanted systems that further differ in data rate requirements. Moreover, the wireless channel conditions inside a body also perform different features from that on the skin surface. Existing possible systems [2, 3] for the WBAN applications, however, provide single modulation scheme that have difficulty meeting the whole application spectrum with unacceptable power consumption. Furthermore, those candidate systems operate at the industry-science-medical (ISM) band may easily be fully occupied by unexpected interference. Accordingly, Federal Communications Committee (FCC) defines a set of wireless medical telemetry service (WMTS) band [4], and our previous proposal [1] was designed under the basis of the WMTS constraints.

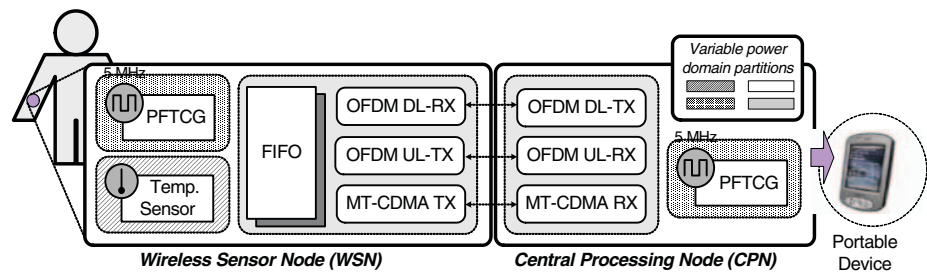
It is necessary to provide a dedicated hardware solution for microwatt WBAN applications. State-of-the-art platforms [5, 6] achieve highly integrated SoC designs with mature FSK wireless scheme. An alternative RF front-end design [7] focuses on a pulse-based radio transmission. Those designs are implemented with above 1 V supply voltage and milli-order power consumption.

The proposed WBAN platform contains a WSN and a CPN that are attached on human body skin and integrated in a portable device, respectively. The system block diagram is illustrated in Fig. 1. A FIFO-based memory is

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Figure 1 The functional blocks of WSN and CPN baseband transceiver.



designed in the WSN that is used to record body signals from internally integrated all-digital smart temperature sensor or other external connected body sensors. The memory size and clocking speed are optimized for and aimed at the electrocardiography signal that are regarded as the most complex signals among body information sources.

Compared to the baseband processing speed, the WSN takes much longer time to record body signals. This results in the WSN-CPN pair staying inactive for most of time and awake in burst for data transmission. The clock sources in the WSN and CPN are implemented by a phase-frequency tunable clock generator (PFTCG). It is used to adjust the generated clock phase and frequency automatically for better system performance and reduced power consumption. Each block in both the WSN and CPN is designed for a specific power-voltage domain for low-power management.

2 System Overview

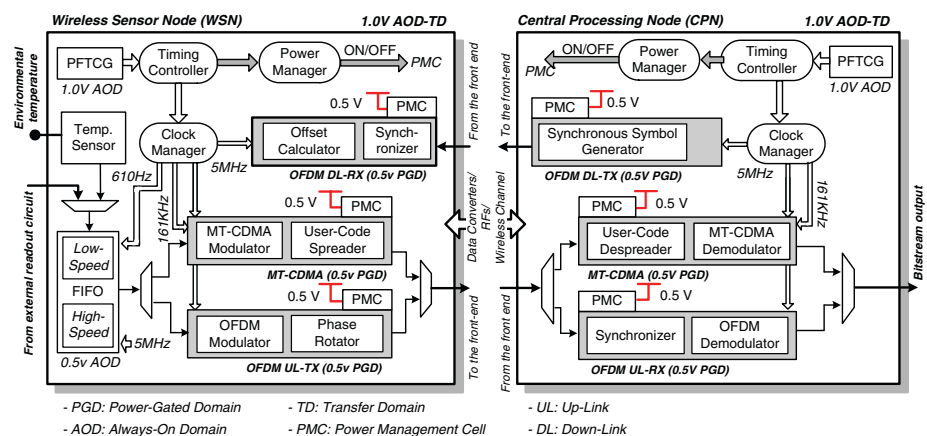
The WBAN transceiver chipset is designed with power-domain partitions for voltage scaling, multi-supply voltage (MSV), and power gating to achieve extreme low power consumption as illustrated in Fig. 2. With the voltage scaling and multi-supply voltage techniques, the system is partitioned into 12 power domains with possible different voltage supplies.

According to the required operating speed and the achievable functionality, the supply voltage 0.5 V is provided globally to every functional block, except special function blocks and transfer-domain (TD) that are operated at 1.0 V to interface with I/O pads. Furthermore, every power domain is not necessary to be activated together. So, the other inactive domains can be switched into sleep phase for most leakage power saving. This active-sleep behavior is achieved by a power management cell (PMC) that contains distributed coarse-grain power gating cells (DCG-PGC) [1] and isolation cells.

The power manager sends commands to the PMC to turn ON/OFF the power-gated domain (PGD). When an OFF signal is asserted, the isolation cell first de-activates by pulling high the signal in the always-on-domain (AOD) side. After that, the DCG-PGC shuts the virtual VDD off. Therefore, the unknown signal from the power-off domain will not affect the other domains. The PMC behavior is in the reverse way when a domain goes to active state. On the other hand, if a hardware block always stays active, its power will not be gated and is referred as always-on domain (AOD).

In addition, the chipset has several clock domains to drive different sequential circuits. For the MT-CDMA block, a clock of 1/31 time of the original frequency is needed. Besides, a low frequency clock to record the body sensor's output is necessary. Therefore, an embedded clock

Figure 2 The detail baseband transceiver block diagram (WSN and CPN).



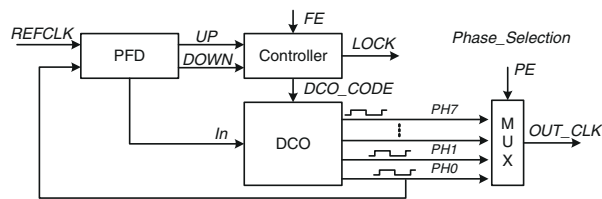


Figure 3 The proposed PFTCG architecture.

generator provides the 5 MHz clock source, and a clock manager unit is designed for frequency synthesis. The synthesized frequency outputs 5 MHz, 161 kHz, and 610 Hz clocks to cover all possible requirements.

There are total three operation modes in the WSN, MT-CDMA TX, OFDM DL-RX, and OFDM UL-TX, to support the dual mode transmission and pre-calibration. First, in the MT-CDMA TX mode, FIFO stores the sensed signals whereas the MT-CDMA transmitter is idled in the sleep phase. When the stored data in low-speed FIFO is full, the MT-CDMA transmitter is waked up to transmit those signals in the active phase. The 161 kHz and 5 MHz clocks are used for modulation and user code spreading respectively.

Second, in the OFDM DL-RX mode, the OFDM receiver is synchronized to the downlink training symbols and calculates the frequency offset for pre-calibration. The 5 MHz clock is used for the OFDM receiver block as well as the OFDM transmitter block.

Lastly, when WSN operates in the OFDM UL-TX mode, the OFDM transmitter can also be separated into two phases. OFDM transmitter is in active phase when transmitting the data and in sleep phase when waiting for the sensed data storing. The frequency offset is pre-calibrated by the digital data distortion and tuning the frequency generated from PFTCG. In these modes, only the corresponding PGD is waked up, the other PGDs are turned off to save the leakage power.

An all-digital smart temperature sensor is integrated in the WSN. The measured temperature data and other

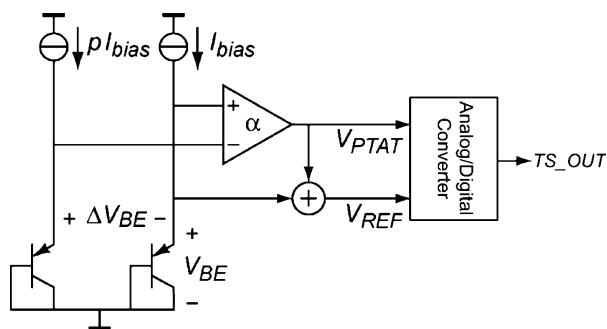


Figure 4 The BJT-based smart temperature sensor.

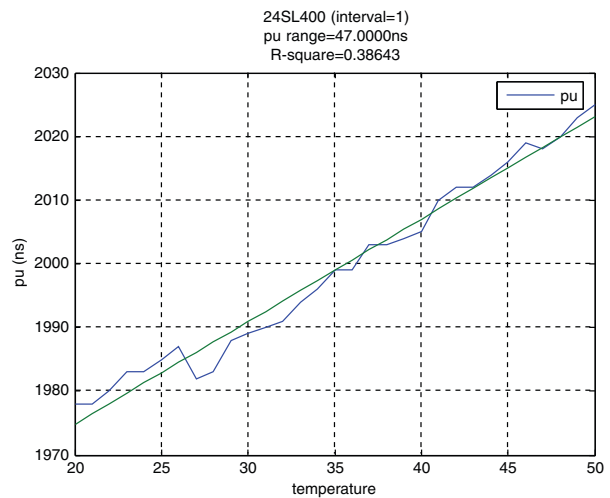


Figure 5 The pulse width of the temperature sensor implemented with 90 nm short-channel MOS devices.

external sensor data are stored in the register-based FIFO. The biomedical signal is highly correlated in time domain so that a FIFO has benefits in the minimum switching power consumption, resulting in both reduced dynamic and leakage power for body-oriented signal storage.

The total size of FIFO is 1024x8 bits that are further equally divided into two banks. One of the FIFO banks is driven by the 610 Hz clock, which is synchronous to the sensor data. The other bank operates at 5 MHz and delivers the data to the baseband modulator. The low speed bank collects data in longer period until it is full. As the content of the low speed bank is full, the bank dumps all its content to the high speed bank and can continue on collecting the data without any loss.

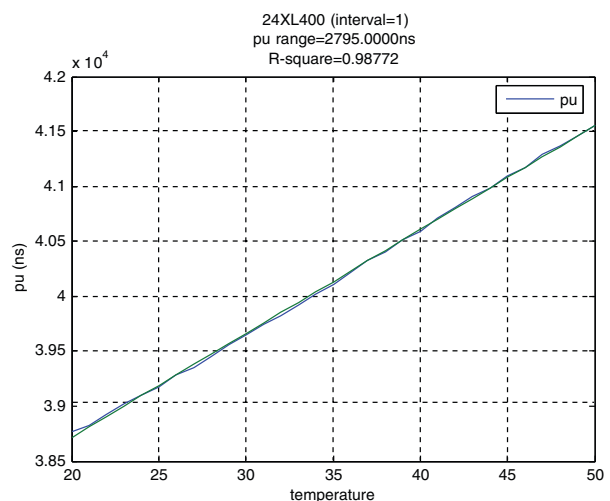


Figure 6 The pulse width of the temperature sensor implemented with 90 nm long-channel MOS devices.

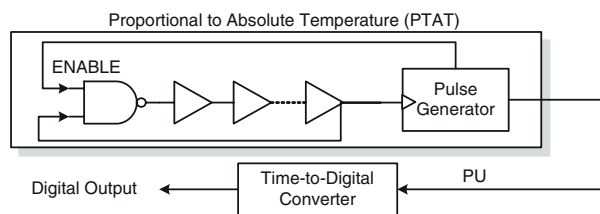


Figure 7 The proposed all-digital smart temperature sensor architecture.

The CPN has three operation modes, MT-CDMA RX, OFDM DL-TX, and OFDM UL-RX, in CPN. First, when CPN operates in the MT-CDMA RX mode, the received data from the front-end is directed to the MT-CDMA receiver block. The data is first de-spread by the 31-chip user code followed by the MT-CDMA demodulator. The synchronizer of MT-CDMA is able to calculate a better sampling phase for the PFTCG. Second, in OFDM DL-TX mode, the OFDM DL-TX broadcasts synchronous symbols and the content of the synchronous symbols is adjustable depending on the user selection. Lastly, in the OFDM UL-RX mode, the received data is switched to the OFDM uplink receiver where the synchronization block is first encountered followed by the OFDM demodulation block.

When CPN is in one of the operation modes, the corresponding PGD is activated and the others are in sleep phase. The rest block of CPN is PFTCG, which generates a 5 MHz clock with eight different phases for synchronization. This clock signal is sent to the clock manager unit, where a 5 MHz clock is bypassed to all the three blocks and a 161 kHz clock is generated for the MT-CDMA demodulator.

The phase-frequency tunable clock generator (PFTCG), as shown in Fig. 3, is designed for performance improvement in WSN and power reduction in CPN. There are four major blocks, including phase-frequency detector (PFD), controller, digitally-controlled oscillator (DCO) and phase selection multiplexer. The PFD generates UP or DOWN commands to modify the frequency of DCO in the tracking loop. When this loop achieves the lock state, the resulting

clock frequency corresponds to the desired 5 MHz clock, which is regarded as the coarse tuning step.

The DCO further generates eight multi-phases as the lock state is reached. It is designed with eight same delay cells, and each delay cell provides $T_{REFCLK}/8$ delay time, resulting in eight equally-spaced multi-phase clock signals between $Cycle_N$ and $Cycle_N+1$. Then one of these 8 sources is selected via the phase-selection. The correct frequency is generated by the closed loop of PFD, controller, and the phase_0 (PH0) in the DCO. This guarantees the resulted clocks keep the same delay spacing $T_{REFCLK}/8$ when the process-voltage-temperature (PVT) condition changes.

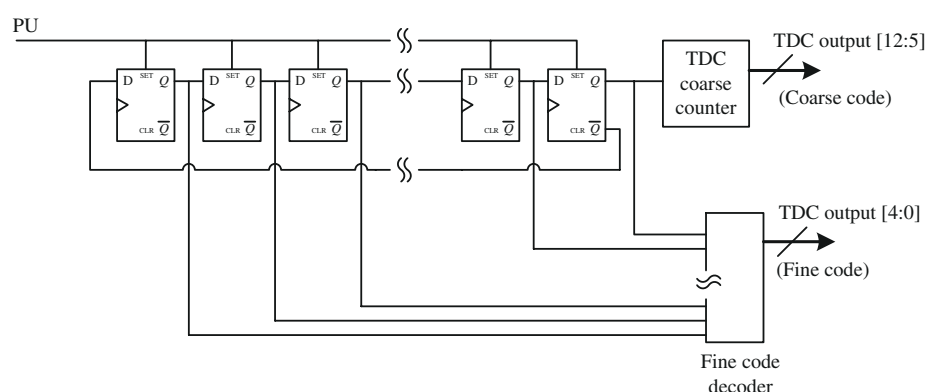
The PFTCG allows the WSN and CPN to slightly change the generated clock frequency and phase by sending a command frequency-error (FE) and phase-error (PE) to the controller and multiplexer, respectively. This frequency fine-tuning capability reduces the sampling clock offset between the WSN and CPN for better performance, and the phase-selection capability enables the CPN to sample incoming signals at better instances without increasing sampling frequency.

3 On-chip Temperature Sensor

The on-chip body temperature sensor for biotelemetry applications must be small area, low-power consumption and easy integration with the transceiver. The temperature sensor should have extreme low-power consumption to avoid self-heating effects to the system, and it must be easy to perform absolute temperature calibration and has sufficient conversion rate to dynamically monitor the body temperature profile.

Traditionally, temperature sensors are built by thermistors or platinum resistors, and require separate readout circuitry. The smart temperature sensor combines sensor and interface electronics into a single chip, and it can be manufactured on the low-cost CMOS process. Hence it becomes more and more popular today.

Figure 8 The proposed time-to-digital converter (TDC).



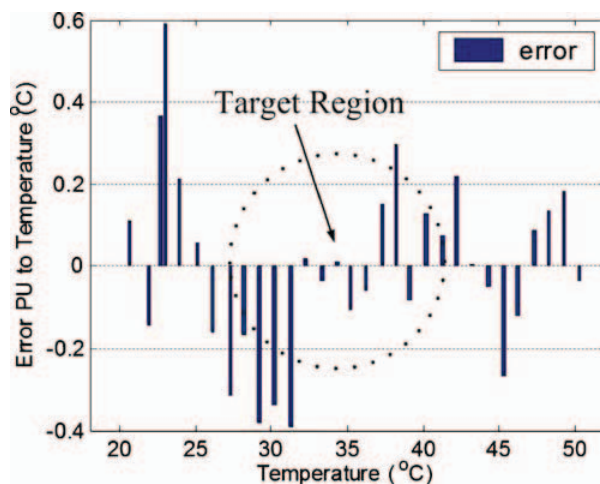


Figure 9 The measurement results of the proposed all-digital smart temperature sensor.

The BJT-based smart temperature sensors are widely used in many applications. Figure 4 shows the concept of BJT-based smart temperature sensors [8]. The temperature sensor generates a voltage (V_{PTAT}) proportional to the absolute temperature. The reference block generates a constant voltage (V_{REF}) which is independent of the temperature within the operation range. Then the analog-to-digital converter (ADC) converts the difference between V_{PTAT} and V_{REF} into a digital code (TS_OUT). However, it is not possible to keep the reference voltage (V_{REF}) constant over the whole temperature range with process and voltage variations. As a result, second order curvature correction circuit, sigma-delta modulator, and post-silicon transistor trimming are used in the sensor [8] to improve the accuracy of temperature measurement. However these calibration circuits increase the circuit complexity and are not suitable for 90 nm process which often with 1.0 V low supply voltage. The total power consumption and chip area are also increased due to the bias circuits and the calibration circuits. And it also takes more efforts to integrate the analog circuits with the digital circuits. As a result, the BJT-based smart temperature sensors are not suitable for on-chip body temperature sensor in biotelemetry applications.

The propagation delay of the delay line can be used to measure the temperature. The delay line-based smart temperature sensor [9] first generates a pulse with a width proportional to the absolute temperature. Then, a cyclic time-to-digital (TDC) converter is utilized to convert this pulse into a corresponding digital code. The advantage of this architecture is that it is a fully digital circuit and is easy integrated with other digital circuits. However the proposed cyclic TDC [9] with pulse-shrinking mechanism takes a long time to convert the pulse width into the digital codes. Therefore the other delay line with low thermal sensitivity is needed to cancel the DC offset and reduce the TDC conversion time. As a result, chip area and power consumption are increased due to the two delay lines architecture.

Figure 5 shows the simulation results of the delay line-based smart temperature sensor implemented with 90 nm short-channel MOS devices. However, the propagation delay is not linearly proportional to the absolute temperature when short-channel MOS devices are used. But if the long-channel MOS devices are used in the delay line circuit, the linearity can be improved as shown in Fig. 6. As a result, in the proposed smart temperature sensor, long-channel MOS devices are used to build up the delay cell of the delay line. And therefore the temperature error due to the nonlinearity of the propagation delay can be reduced.

Figure 7 shows the architecture of the proposed all-digital temperature sensor. To reduce chip area and enhance resolution of the digital read-out circuit, a cyclic delay line with a pulse generator is used to generate a long duration pulse. The cyclic delay line is a temperature-to-pulse generator. It is used to generate a pulse and its width is proportional to the absolute temperature (PTAT). The delay cells in the cyclic delay line are built with the long-channel MOS devices. The pulse generator counts the positive edge triggers from the cyclic delay line, and when a specified value N is reached in the counter, the cyclic delay line is stopped. Then the pulse width of the output signal “PU” becomes $N \times T_d$, where T_d means the period of cyclic delay line’s output, and the time-to-digital converter (TDC) is utilized to quantize the pulse width of “PU” into the digital codes.

Table 1 Comparisons of recent smart temperature sensor.

Sensor	Error (°C)	Power	Area (mm ²)	Conversion Rate (samples/sec)	Temperature Range (°C)	CMOS Technology
[8]	±0.1 (3σ)	247 μW@ 3.3 V	4.5	10	−55~125	0.7 μm
[9]	−0.7~+0.9	0.49 mW@ 3.3 V	0.175	1,000	0~100	0.35 μm
[10]	−1.8~+2.3	12 mW@ 1.2 V	0.16	5,000	0~100	0.13 μm
proposed	±0.6	0.38 mW@ 1.0 V	0.12	1,000	20~50	90 nm

Figure 10 The current profile between sleep and active modes.

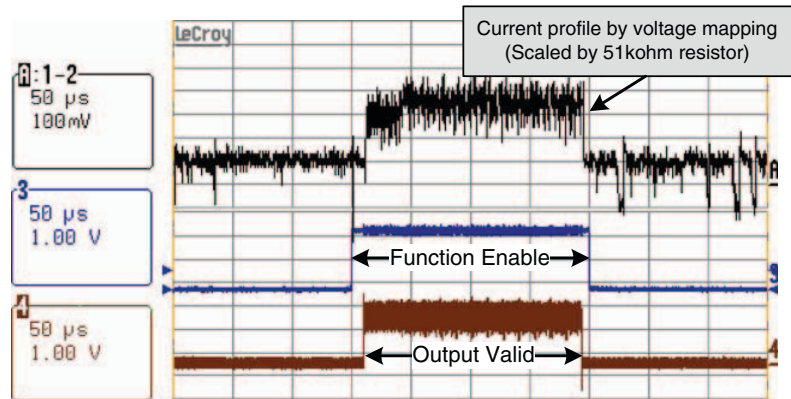


Figure 8 shows the architecture of the proposed TDC. The TDC is composed of the coarse counter and the fine code decoder to achieve high resolution quantization. In the proposed TDC, 16 latches are used to compose the TDC cell line. When the signal “PU” outputted from the pulse generator is enabled, then all latches in the TDC cell line are turned on and the TDC cell line starts to oscillate. The TDC’s coarse counter counts the arrival positive edges to generate the TDC coarse code. This operation is continued until the signal “PU” is disabled. Then the residual pulse width information can be generated after the fine code decoder. And the output of the TDC coarse counter and the fine code decoder are combined as the TDC_output[12:0]. The resolution of the TDC is limited by the propagation delay of the TDC cell line and the setup/hold time requirements of the latches. As a result, the TDC must perform simulation with PVT variations to make sure that the output temperature error are not mainly comes from the TDC. Then we can get the absolute temperature information after one-point or two-point temperature calibration during chip measurement.

4 Experimental Results

The proposed all-digital smart temperature sensor with WBAN baseband transceiver chipset is fabricated on a standard 90 nm 1P9M CMOS process. Figure 9 shows the measured temperature error of the proposed temperature sensor. This temperature sensor is designed for human body temperature measurement in the range from 35°C to 40°C. The proposed design performs good linearity in this range and achieves error < 0.6°C.

Table 1 lists the comparisons of recent smart temperature sensors. In BJT-based smart temperature sensor [8], the sensor has large chip area because of the complex calibration circuits. And this sensor can only achieve a maximum conversion rate at 10 samples/sec. In the all-digital smart temperature sensors [9, 10], the proposed design can achieve higher conversion rate with lower power consumption. And the two-point temperature calibration is performed in the proposed design. Although the temperature error is very small ($\pm 0.1^\circ\text{C}$) in [8], this BJT-based temperature sensor is not suitable for on-chip body

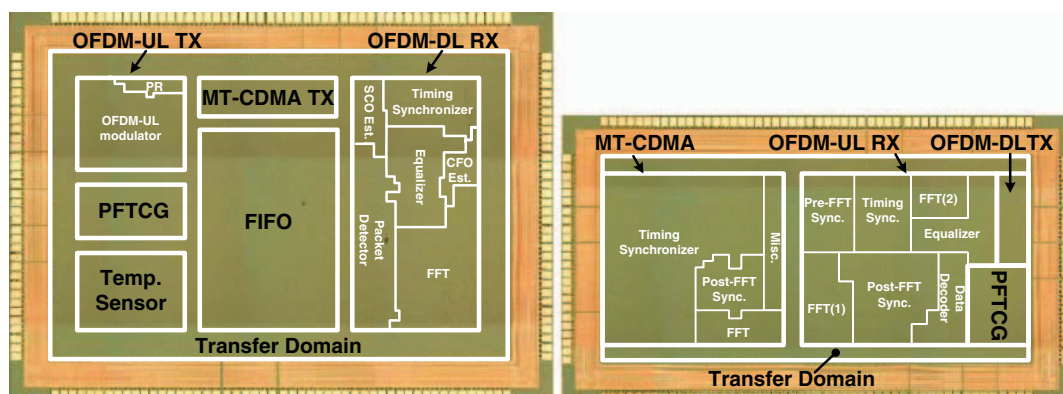


Figure 11 The microphotograph of WSN and CPN.

temperature sensor in biotelemetry applications. And in [10], the high power consumption and large chip area makes it is also not suitable for biotelemetry applications.

The power-domain of this chip is turned on by the DCG-PGC. The OFDM DL-TX building block is used for the illustration of the current profile between active and sleep states. This current profile is generated by concatenating a resistor (51 k ohm) in the way of core power path for clear instrument observation, and the voltage between this resistor's two sides is shown in Fig. 10. As the ENABLE signal is activated, the OFDM DL-TX domain is turned on, and more current is drawn that corresponds to μ -level power consumption.

This WBAN transceiver improves the system data rate from 143 kbps to 7 Mbps. This largely reduces the system working duty cycle (i.e. the percentage of circuit active time). The transmission energy is reduced from previous proposal 21 μ W [1] to this work 5.52 μ W, resulting in 73.7% efficiency improvement in baseband circuit processing. Figure 11 shows the micro chip photos. Each bold-rectangular denotes a separate power domain with the rest region as the transfer domain for I/O-pad interfaces.

5 Conclusions

This work provides an all-digital smart temperature sensor with dual-mode baseband transceiver chipset for wireless body area network (WBAN). The proposed delay line-based all-digital smart temperature sensor implemented with long-channel MOS devices achieves good linearity in temperature measurement. A clock generator with frequency and phase tuning capability is provided for system performance improvement and power reduction. The supply voltage is scaled to 0.5 V with dedicated power-domain partitions. The power efficiency is improved in baseband signal processing. As a result, this work provides an extreme low-power and highly-integrated WBAN platform, especially suitable for the biotelemetry applications.

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